D.Module2.AD25M16

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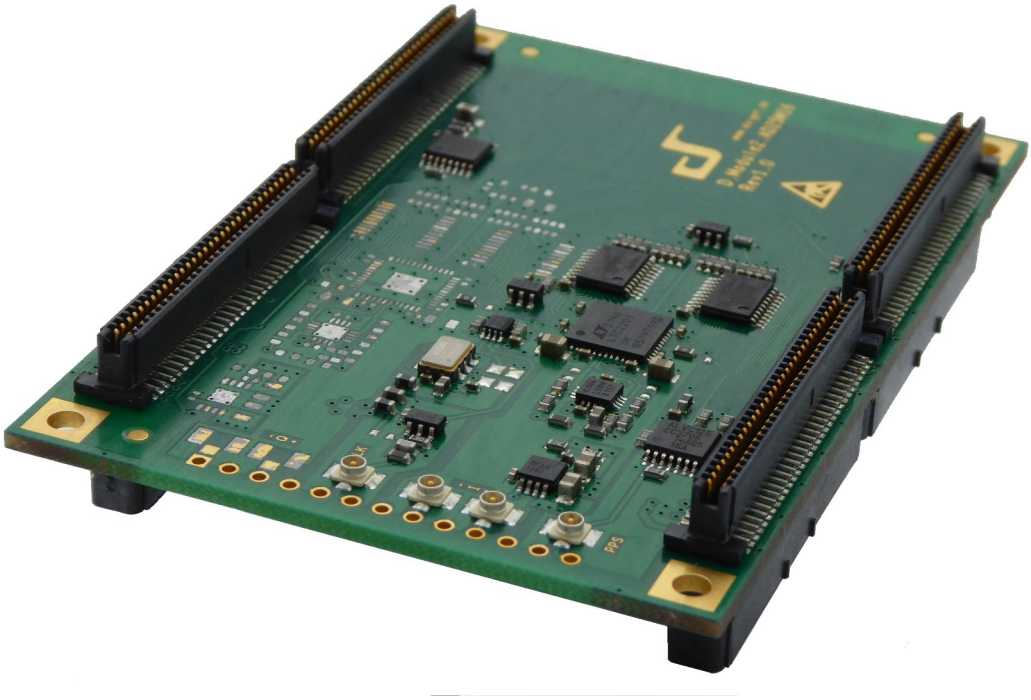
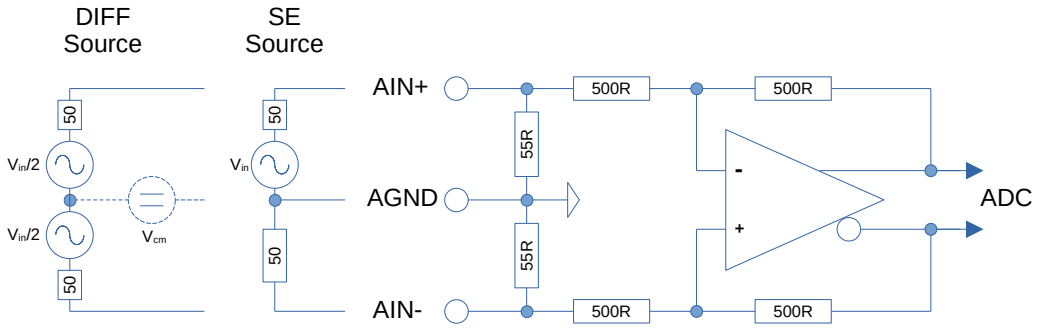


Key Features

- Two differential analog inputs
- Simultaneous sampling up to 25 MSps
- Internal or external sampling clock
- 16-bit resolution
- Time-stamping and sampling frequency locking with external PPS reference pulse
- Synchronous parallel data ports, I²C control interface
- 200 MHz analog input bandwidth supports subsampling applications

The D.Module2.AD25M16 is a data acquisition daughter card for the D.Module2 DSP and FPGA boards. It features two LTC2203 A/D converters, two LTC6403 analog frontends and a programmable SI514 oscillator to generate the sampling clock. The digitized data is provided to the DSP/FPGA via two 16-bit uPP interface channels. The AD25M16 is also available in a Single-Channel OEM version.

Analog Inputs



The two input channels, named I- and Q-channel, are DC-coupled and 50-ohms terminated. Bipolar single-ended and differential signals with 1.67 or 2.5Vpp amplitude and 50-ohms source impedance are accepted. Single-ended configurations use the AIN+ input and terminate AIN- with an external 50 ohms resistor. Differential configurations accept a common mode voltage in the -2.5 to +5V range. OEM customers can order the AD25M16 with different gain and termination options, please contact support@dsignt.de

No anti-aliasing filter is provided. A first-order lowpass with 44 MHz cut-off frequency following the input stage prevents excessive high-frequency noise from entering the ADC. This filter can be bypassed for sub-sampling applications, retaining the full 200 MHz analog bandwidth.

ADC

The LTC2203 analog-to-digital converter features a built-in programmable gain amplifier (PGA) which selects the $1.67V_{pp}$ or $2.5V_{pp}$ full-scale input range. The range is software-selected via the I²C control interface. Best performance is achieved in the 2.5V range, the 1.67V range will typically cause a 2dB signal-to-noise ratio loss.

To improve the resolution when measuring very low signal levels an internal dither source can be applied to the ADC. Dithering will raise the noise floor by approximately 0.5dB, but the spurious free dynamic range will improve by 10dB. The dither function is enabled or disabled by software via I²C.

The ADC pipeline architecture delays the digitized samples by 7 sampling clocks. This delay must be compensated if the ADC data is to be time-aligned with other external events.

Power Supply

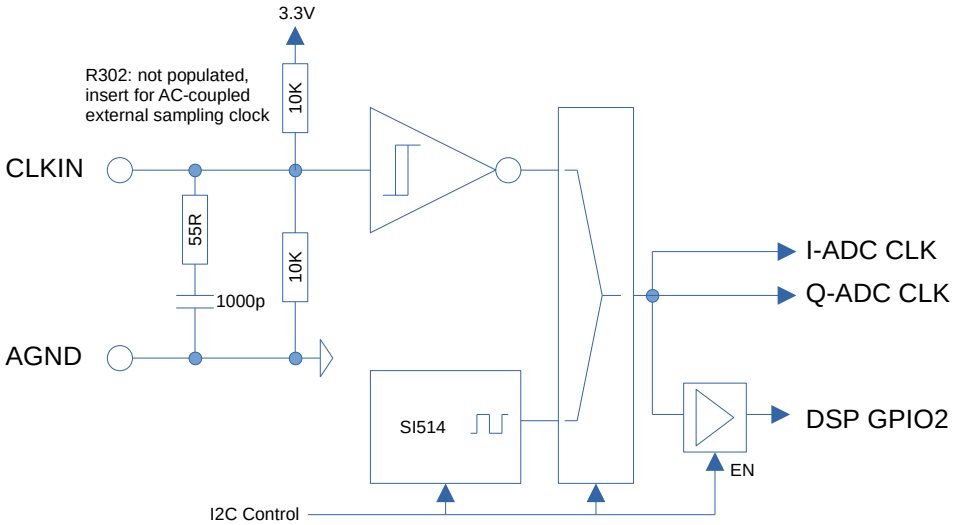
The D.Module2.AD25M16 requires separate analog and digital power supplies. The digital logic operates on 3.3V ±5% and is typically supplied by the attached DSP board via the VCCOUT and GNDOUT pins. If the AD25M16 is not stacked with a DSP board, the digital power supply must be connected to the BUS1 or BUS2 connector pins VCC and GND.

The analog circuits must be powered by a 5V ±10% supply, connected to the BUS1 or BUS2 connector pins AVPOS and AGND. Route the analog power supply to only one of these connectors, whichever best suits the carrier board layout. Digital and analog grounds are joined on the D.Module2.AD25M16. Switch mode regulators are acceptable for the analog power supply. The AD25M16 includes high bandwidth, low noise, linear voltage regulators in the analog power rail which will reject most switching transients. However, power traces must be carefully routed to avoid any inductive or capacitive coupling into the analog and the clock inputs.

A shutdown down mode to minimize the power consumption during idle times is controlled via the I²C interface.

Sampling Clock

The sampling clock can be generated internally by a programmable SI514 oscillator or applied externally. The valid range is 1 to 25 MHz. The external clock input accepts a single-ended LVTTL signal (Low < 0.4V, High > 2V). A sinusoidal AC-coupled clock can be used if an additional resistor is populated on the AD25M16 board. The ADC will start a conversion on each rising CLKIN edge. The sampling clock is fed to both ADCs and optionally to the DSP board GPIO2 input to be used as a timer clock source.



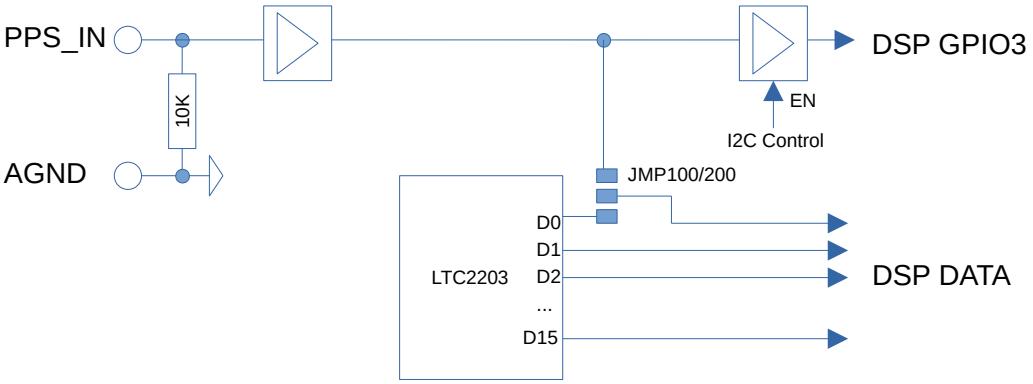
Timestamps and Frequency Locking

If the analog data acquisition requires precise time-stamping, a reference signal, e.g. a PPS (pulse per second), can be stored with the digitized data. The AD25M16 provides a PPS_IN LVTTL input. Of course any frequency reference other than a PPS pulse can be applied too. The available options are:

1) if only one analog input is required the Q-channel can be used to sample the reference pulse. The single-channel version AD25M16-1 leaves the Q-channel analog frontend and ADC unpopulated and routes the PPS_IN input to the Q-channel data bit Q_D0.

2) In a dual-channel system the ADC LSB data bit I_D0 or Q_D0 can be replaced with the PPS_IN signal. This only slightly degrades the analog performance. The DSP must either mask this PPS bit or replace it with a random value before the analog data is processed further. Jumper J100 (I-channel) and J200 (Q-channel) determine whether the ADC converter LSB or the PPS_IN input is routed to the data bit 0 output.

3) PPS_IN can be switched to the DSP GPIO3 input to be used as an interrupt or timer source.



Keep in mind that the ADC pipeline architecture delays the digitized output by 7 sampling periods. PPS_IN however is sampled directly without delay. A PPS_IN event is therefore time-aligned with the ADC data arriving 7 sampling clocks later.

When using the SI514 on-board oscillator the sampling frequency can be locked to the PPS reference signal. The SI514 provides sub-ppb (parts-per-billion) frequency resolution and can be pulled +/- 1000 ppm from the programmed frequency without interrupting the clock. To lock the sampling frequency to the PPS reference the DSP counts the number of samples received between two PPS pulses and applies a correction factor to the SI514 oscillator. Example: target sampling frequency is 25 MHz, DSP received 24.9995 million samples between two PPS events → pull SI514 by 1e6 * (25e6 – 24.9995e6) / 25e6 ppm = +20ppm.

I²C Control Interface

The configuration of the AD25M16 board is done via I²C transfers. The AD25M16 uses the following I2C devices:

SI514 programmable oscillator, slave address 0x58

PCA 9554A 8-bit port expander, slave address 0x38, all port pins configured as output

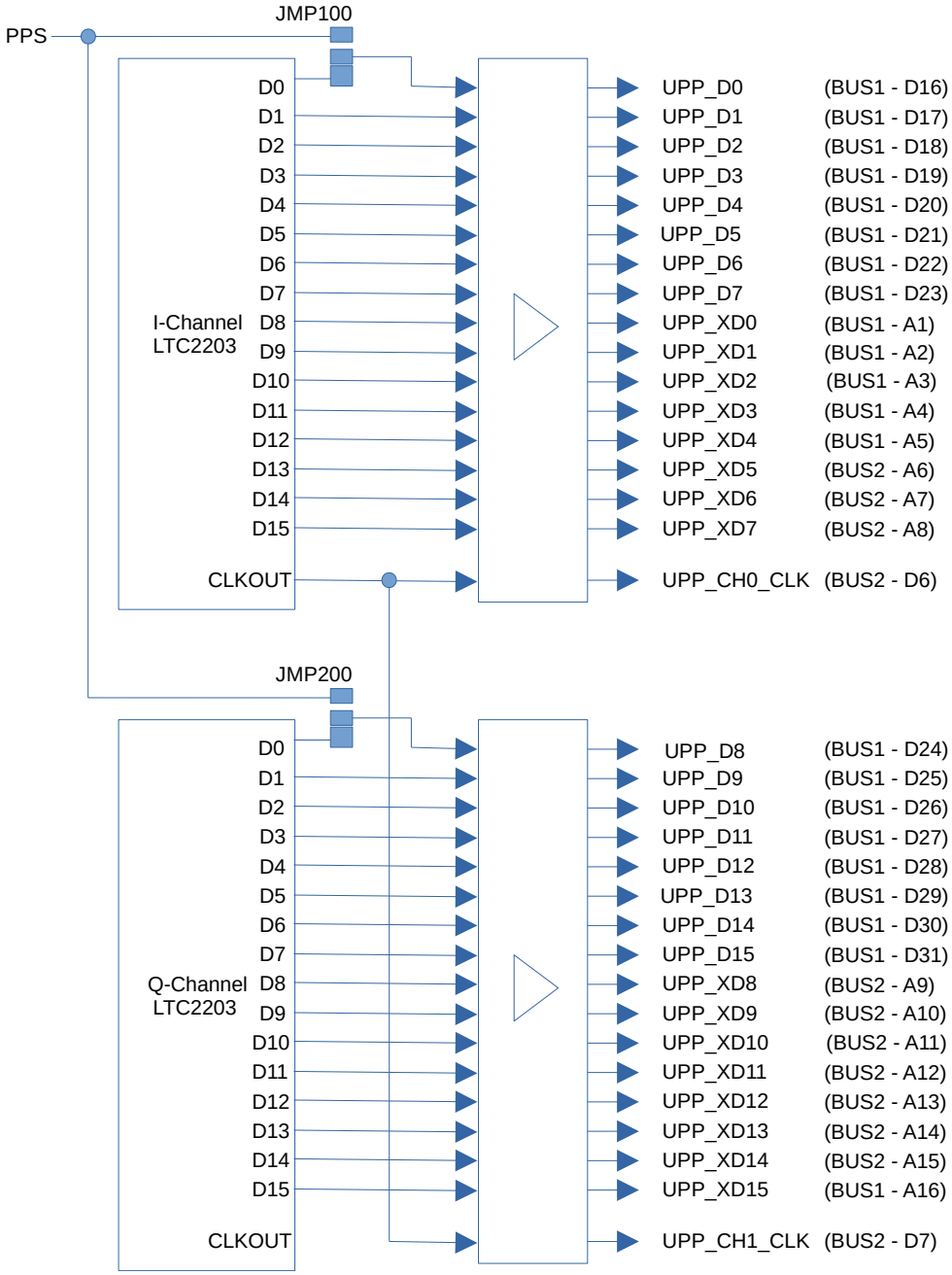
Bit 0 – SHDN	0: normal operation, 1: board in power-save mode
Bit 1 – SHDN#	must be Bit 0 (SHDN) negated
Bit 2 – PGA	0: 2.5V input range, 1: 1.67V input range
Bit 3 – DITH	0: Dither disabled, 1: Dither enabled
Bit 4 – reserved	always write 0
Bit 5 – CLKSRC	0: external sampling clock, 1: SI514 generates sampling clock
Bit 6 – GPIO2_CLK	0: GPIO2 unused (high impedance), 1: Sampling Clock connected to GPIO2
Bit 7 – GPIO3_PPS	1: GPIO3 unused (high impedance), 1: PPS_IN connected to GPIO3

Make sure to avoid address conflicts in systems where additional external slave devices are connected to the I²C bus.

Databus Interface

The digital data outputs and the clock outputs of the I and Q channel ADCs are buffered and connected to the DSP uPP synchronous parallel interface. Data is read by the DSP on the rising clock edge.

On the D.Module2 the uPP port signals share pins with the external bus interface. The DSP board must be configured to uPP bus mode to use the AD25M16 daughter card. The uPP signals WAIT, START and ENABLE are not used by the AD25M16 and must be de-activated in the DSP uPP configuration.



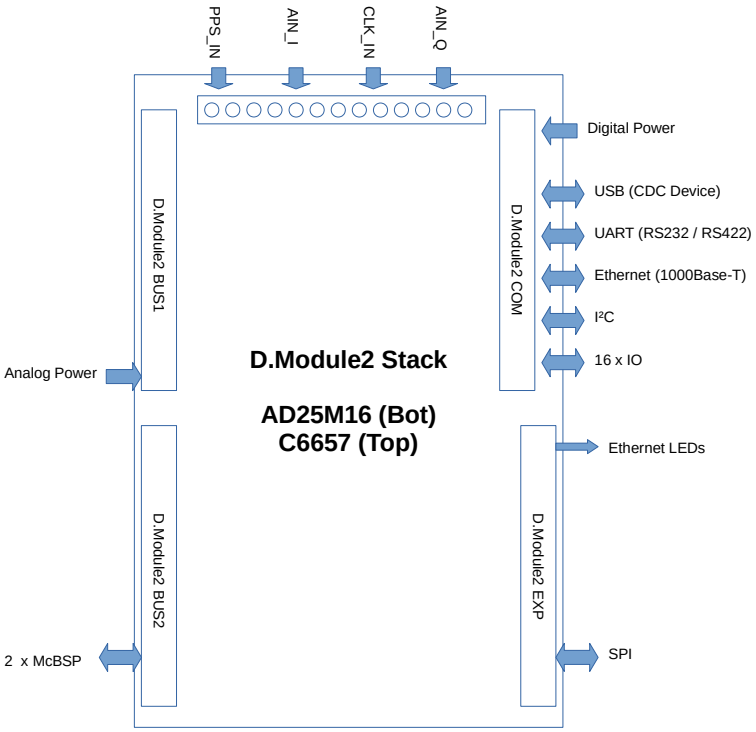
System Interface

The analog inputs, the external sampling clock input, and the PPS timestamp input are all available on a 13-pin, single-row, 2.54mm pitch connector and additionally on six miniature Hirose U.FL coaxial connectors. A straight 13-pin connector can be used to route these signals to a carrier board. Alternatively U.FL cables can be used for best shielding and signal integrity.

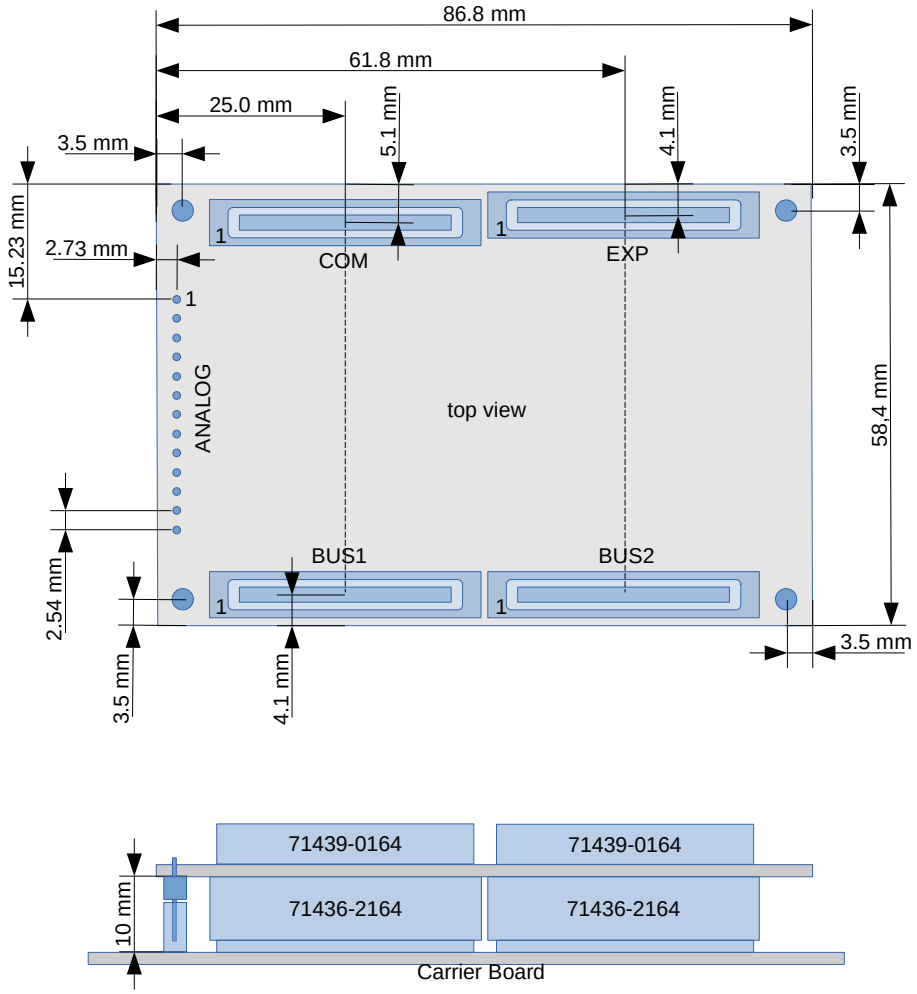
The DSP interface uses the D.Module2 standard connectors. In a module stack the DSP board must always be mounted on top of the AD25M16. Stacking the boards accomplishes all required interconnections between the DSP board and the AD25M16. All DSP board signals are routed through the AD25M16 board and are available on the carrier board.

> Although possible, stacking is only recommended for functional verification and limited spectral resolution requirements. The high-speed DSP or FPGA board will inevitably radiate high frequency noise into the AD25M16 frontend which is aliased into the baseband, causing artifacts up to -80dB below fullscale. For best performance the AD25M16 should be mounted aside the processor board. All required interconnections must be provided on the carrier board and all power supply and digital signals and associated return paths (GND) must be carefully routed to minimize the enclosed loop area.

The following diagram shows the available interfaces and connections of a D.Module2 stack with C6657 DSP and AD25M16:

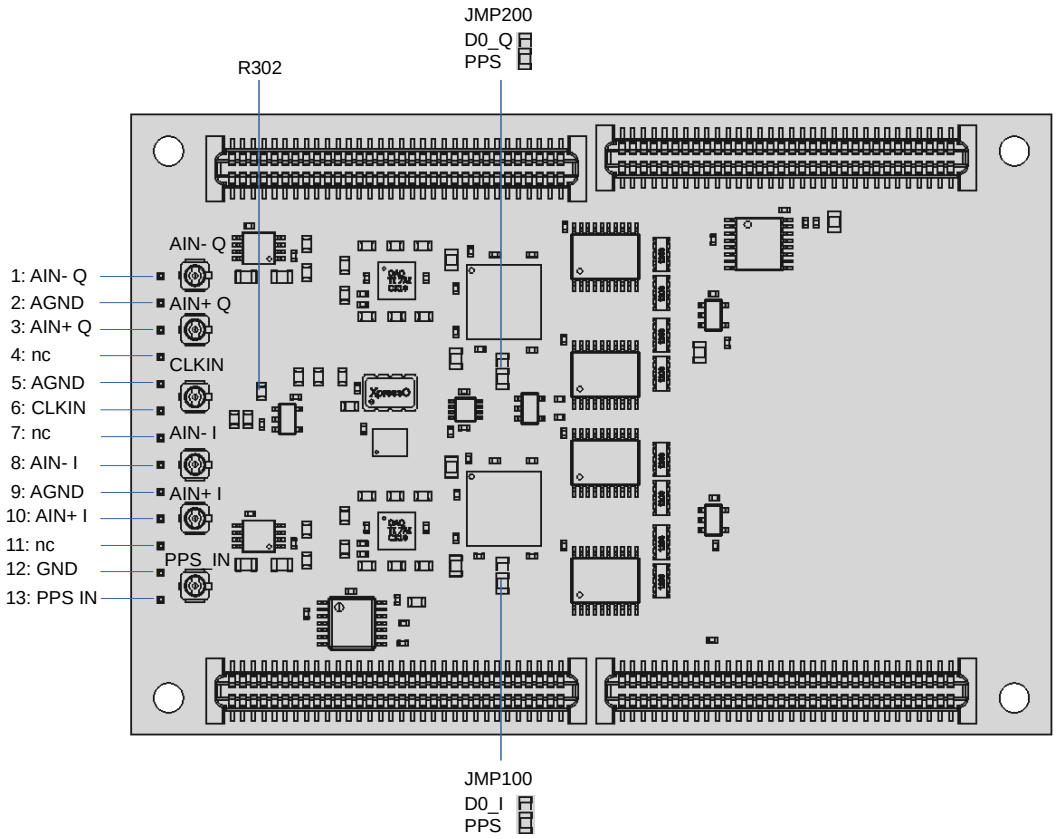


Mechanical Dimensions



Mating carrier board connectors:
4 x Molex 71439-0164 (COM, EXP, BUS1, BUS2)
1 x FCI 75915-313LF or similar (ANALOG)

Location of Analog Inputs and Configuration Jumpers



Connector Pinout

Connector and Pin	Signal	Description
ANALOG – 1	AIN-Q	Q-Channel inverting analog input
ANALOG – 2	AGND	Q-Channel analog GND
ANALOG – 3	AIN+Q	Q-Channel non-inverting analog input
ANALOG – 5	AGND	External sampling clock analog GND
ANALOG – 6	CLKIN	External sampling clock input
ANALOG – 8	AIN-I	I-Channel inverting analog input
ANALOG – 9	AGND	I-Channel analog GND
ANALOG – 10	AIN+I	I-Channel non-inverting analog input
ANALOG – 12	GND	PPS GND
ANALOG – 13	PPS_IN	PPS reference input

Connector and Pin	Signal	Description
BUS1 – 1, 2	VCC	Digital Power Supply 3.3V
BUS1 – 3, 4	GND	Digital Power Supply 0V
BUS1 – 23	I_D8	I-Channel Data Bit 8
BUS1 – 25	I_D9	I-Channel Data Bit 9
BUS1 – 26	I_D10	I-Channel Data Bit 10
BUS1 – 28	I_D11	I-Channel Data Bit 11
BUS1 – 29	I_D12	I-Channel Data Bit 12
BUS1 – 30	Q_D15	Q-Channel Data Bit 15
BUS1 – 36	I_D0	I-Channel Data Bit 0
BUS1 – 37	I_D1	I-Channel Data Bit 1
BUS1 – 38	I_D2	I-Channel Data Bit 2
BUS1 – 39	I_D3	I-Channel Data Bit 3
BUS1 – 41	I_D4	I-Channel Data Bit 4
BUS1 – 42	I_D5	I-Channel Data Bit 5
BUS1 – 44	I_D6	I-Channel Data Bit 6
BUS1 – 45	I_D7	I-Channel Data Bit 7
BUS1 – 46	Q_D0	Q-Channel Data Bit 0
BUS1 – 47	Q_D1	Q-Channel Data Bit 1
BUS1 – 49	Q_D2	Q-Channel Data Bit 2
BUS1 – 50	Q_D3	Q-Channel Data Bit 3
BUS1 – 52	Q_D4	Q-Channel Data Bit 4
BUS1 – 53	Q_D5	Q-Channel Data Bit 5
BUS1 – 54	Q_D6	Q-Channel Data Bit 6
BUS1 – 55	Q_D7	Q-Channel Data Bit 7
BUS1 – 59, 60	AGND	Analog Power Supply 0V, internally connected to GND
BUS1 – 61, 62	AVPOS	Analog Power Supply +5V
BUS1 – 8, 11, 16, 19, 24, 27, 32, 35, 40, 43, 48, 51	SGND	Signal Return GND, internally connected to GND

Connector and Pin	Signal	Description
BUS2 – 3, 4	AVPOS	Analog Power Supply +5V
BUS2 – 5, 6	AGND	Analog Power Supply 0V, internally connected to GND
BUS2 – 7	GPIO2	Unused (high impedance) or Sampling Clock Output to DSP
BUS2 – 8	GPIO3	Unused (high impedance) or PPS Output to DSP
BUS1 – 16	I_CLK	I-Channel Data Clock
BUS1 – 17	Q_CLK	Q-Channel Data Clock
BUS1 – 30	I_D13	I-Channel Data Bit 13
BUS1 – 31	I_D14	I-Channel Data Bit 14
BUS1 – 32	I_D15	I-Channel Data Bit 15
BUS1 – 33	Q_D8	Q-Channel Data Bit 8
BUS1 – 35	Q_D9	Q-Channel Data Bit 9
BUS1 – 36	Q_D10	Q-Channel Data Bit 10
BUS1 – 38	Q_D11	Q-Channel Data Bit 11
BUS1 – 39	Q_D12	Q-Channel Data Bit 12
BUS1 – 40	Q_D13	Q-Channel Data Bit 13
BUS1 – 41	Q_D14	Q-Channel Data Bit 14
BUS1 – 61, 62	GND	Digital Power Supply 0V
BUS1 – 63, 64	VCC	Digital Power Supply 3.3V
BUS1 – 13, 18, 21, 26, 29, 34, 37, 42, 45, 50, 53	SGND	Signal Return GND, internally connected to GND

Connector and Pin	Signal	Description
COM1 - 37	SCL	I2C Interface Clock
COM1 - 38	SDA	I2C Interface Data
COM1 – 35, 36	SGND	I2C Interface signal return GND, internally connected to GND

Electrical Characteristics

Analog Inputs	2, single-ended or differential, DC-coupled bipolar input range programmable 1,67V_{pp} or 2.5V_{pp} fullscale common mode voltage (differential input only): max. -2.5V to +5V input impedance 50Ω -3dB bandwidth 44 MHz, option: 200 MHz RMS wideband idle noise: -81dBFS @ 25Msps
A/D Converter	2, LTC2203 resolution 16 bit sampling frequency 1 MHz to 25 MHz delay analog input to digital data: 7 sampling periods
Sampling Clock	internally generated by SI514 oscillator or externally supplied via CLKIN, LVTTL level (sinewave with AC-coupling)
Timestamp Reference	externally supplied PPS pulse, LVTTL level
Power Supply	digital: 3.3V ±5%, typ. 30 mA, max. 50 mA analog: 5V ±10%, typ. 150 mA, max. 250 mA
Data Interface	uPP, D.Module2.Bus compatible 2 x 16-bit synchronous parallel interface, LVTTL data format: 2's complement
Control Interface	I²C, max. 400 kBit/s
Temperature Range	-40 .. +85°C
Mating DSP Boards	D.Module2.C6657 D.Module2.C6747 via D.Module2.6SLX45T FPGA

Ordering Information

D.Module2.AD25M16	Dual-Channel ADC board
D.Module2.AD25M16-1	Single-Channel ADC board
DK.C6657i-AD25M16-1	Development Support Kit C6657 and single-channel AD25M16

D.SignT GmbH & Co. KG
phone: +49 (0) 2833 / 570977 • fax: +49 (0) 2833 / 3328
mail: info@dsignt.de • web: www.dsignt.de
Marktstraße 10 • 47647 Kerken • Germany