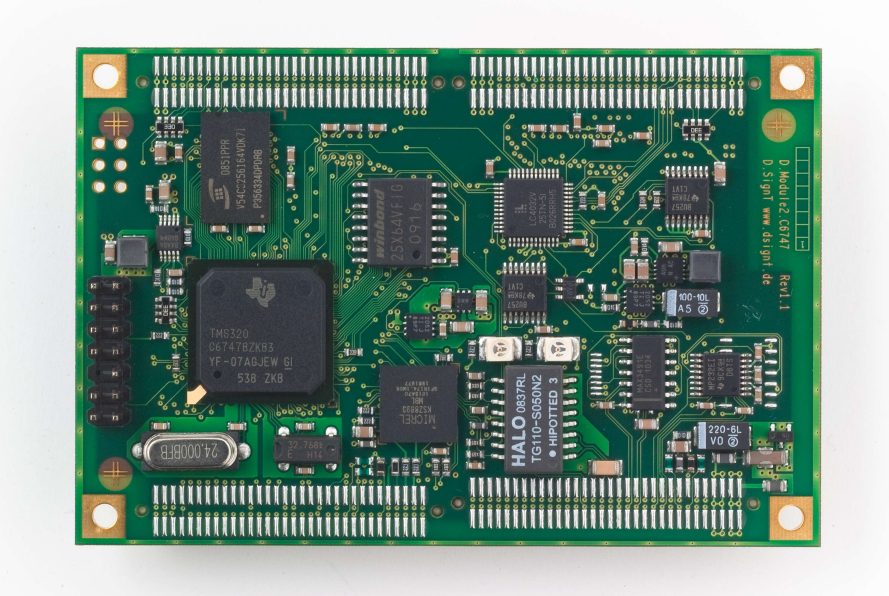
D.Module2.C6747 Technical Data Sheet

Board Revision 1.0 **Document Rev. 1.03** **Nov/2014**

KEY FEATURES

- **300 MHz TMS320C6747 processor optional OMAP-L137**
- **100/10 MBit Ethernet with 2-Port Switch**
- **USB1.1 Host and High Speed USB2.0 Device/OTG**
- **64M Bytes SDRAM**
- **16/32 bit Asynchronous External Bus Interface**
- **8M Bytes non-volatile Flash Memory , optional additional 2G Bytes NAND Flash**
- **Two UARTs, RS232 and RS422/485**
- **Two Multi-Channel Serial Ports**
- **I²C and SPI Interface**
- **SD/MMC Interface**
- **Timer, PWM Outputs, Capture/Compare Unit, Quadrature Encoder Inputs**
- **3.3V single-supply, Supervisor and Watchdog, Real-Time Clock**
- **D.Module2.BIOS programming support for all on-board resources, USB / RS232-based Setup Utility for convenient field-maintenance**



The D.Module2 series represents the next generation of high-performance,stand-alone DSP boards. The self-stacking design allows to build complete signal processing systems by stacking the required DSP, I/O, and data acquisition modules. If data preprocessing is needed, an FPGA module can be inserted between data acquisition and DSP.

The TMS320C6747 is the successor of the popular C6713 floating point processor. The core architecture and instruction set has been enhanced with C64+ features. The L1 program and data caches have been expanded to 32K bytes each. Additionally 256K bytes L2RAM can be configured as direct-mapped memory or as Level-2 cache. The internal memory is further expanded with a 128K bytes shared RAM. Optionally the board can be populated with the OMAP-L137 with an additional ARM9 core on-chip.

The D.Module2.C6747 adds 64M Bytes SDRAM and 8M Bytes non-volatile serial Flash Memory. The non-volatile memory can be expanded by an optional 2G Bytes NAND Flash (see ordering options) and by externally connected MMC/SD Cards.

Data Acquisition Peripherals are interfaced either serially via the two multi-channel serial ports, or via a 16/32-bit wide parallel bus interface.

The C6747 features a rich set of on-chip peripherals: Ethernet, two USB Controllers (1.1 host and 2.0 OTG), two UARTs, Real-Time Clock, PWM outputs, Capture/Compare Timers, Quadrature Encoder Inputs, and I²C and SPI interfaces. The D,Module2.C6747 adds a 2-port managed Ethernet Switch, an additional 16-bit timer and 16 pin-programmable I/O ports.

The high-speed design required special care for signal integrity and EMC. The PCB uses auxiliary GND planes to shield signals and provide controlled impedance signal paths, the power supply lines are extensively filtered, and the connector pinout provides ample signal return ground connections.

Programming support for all on-board peripherals is provided by the D.Module2.BIOS, a set of functions resident in the module's Flash Memory, covering initialization, configuration, and data transfer. Hardware dependencies are encapsulated by the BIOS, hence no software adaptations due to peripheral component or silicon revision changes are required in the user and application programs.

A Setup Utility, also resident in the Flash Memory, provides straightforward field maintenance via USB or RS232: data and program upload, configuration changes, and basic debugging functionality are available without the need for special emulator or programming equipment.

PROCESSOR

TMS320C6747 – 300MHz C67+ core, 2400 MIPS, 1800 MFLOPS. Optionally (OMAP-L137) additional 300 MHz ARM926EJ core.

The 6747 provides on-chip 32K Bytes L1 data cache and 32K Bytes program cache. 256K Bytes L2RAM, configurable as direct-mapped memory or 2-way, 3-way, or 4-way L2-cache, and 128K Bytes shared memory.

The 6747 features two enhanced DMA transfer controllers with 32 independent DMA channels and 8 quick DMA channels for peripheral-memory and memory-memory data transfers.

The on-board peripherals are described later in this document. Please note that due to pin-multiplexing on the C6747 processor not all peripherals are accessible simultaneously. Please refer to the restrictions notes for the affected peripheral.

SDRAM

64M Bytes 32-bit wide SDRAM operates at 133 MHz and provides a throughput up to 500M Bytes/sec. The advanced L1 and L2 cache architecture further enhances memory performance.

FLASH MEMORY

8M Bytes non-volatile serial Flash Memory provide storage for application programs, user data, and configuration settings. The Flash Memory also stores the board's hardware settings, the D.Module2.BIOS API functions, and the Setup and Recovery Utility programs. The D.Module2.BIOS functions provide erase, (block)write and (block)read functions, and a function to program the Flash with Intel-Hex files. The bootload function loads and executes programs stored in the Flash Memory.

Two boot sectors are hardware write protected. These sectors hold the module hardware configuration and the Recovery utility program. Even in case the flash memory is completely erased or overwritten by accident, these sectors remain intact and allow to recover the D.Module2.BIOS and the application without any special programming equipment.

As an option additional 2G Bytes of NAND-Flash is available. If the non-volatile memory needs to be expanded even further, the SD/MMC Card interface can be used.

EXTERNAL BUS INTERFACE

The bus interface is used to connect external peripherals like data acquisition boards or FPGAs.. It is configurable to 16 or 32-bit asynchronous mode. The bus timing is widely programmable. External device can request additional wait states via the WAIT_N input. Up to 50M bytes/sec. throughput can be achieved.

The bus interface uses a 16/32 bit wide data bus. Three external interrupt or DMA request inputs are provided. Four GPIO signals are configurable in the Board Configuration Register and allow to route DSP Timer and/or GPIO signals to external peripherals. Two pre-decoded memory areas are available, which can be individually configured to different data formats and timings.

The bus drivers source/sink up to 24mA and are able to drive long signal lines with passive or active termination.

Note: The external bus interface shares pins with the SD/MMC card interface. Simultaneous access to both functions is not possible. A SW-controlled multiplexer on the D.-Module2 switches between SD/MMC and External Bus Interface.
The 6747 LCD controller interface and the host port interface also share pins with the external bus interface and are not supported on the D.Module2.C6747

ETHERNET

A 10/100 MBit IEEE 802.3 EMAC is built into the 6747 processor. The D.Module2.C6747 adds a PHY with integrated 2-port manageable switch and on-board magnetics for port 0. Port 1 can be used with external magnetics or with a Fiber-optical transceiver.

USB

The 6747 provides both an on-chip USB1.1 OHCI host controller and PHY, and an USB2.0 OTG controller and PHY. USB1.1 is capable of 12 MBit/sec transfer rate, the USB2.0 controller supports up to 480MBit/sec. Bulk, Interrupt and isochronous transfers are supported. The D.Module2.BIOS greatly simplifies USB communications by providing a predefined interface with up to four user-definable endpoints. An on-board boost converter and switches are provided for host and OTG 5V power supply.

UART

Two UARTs with RS232 and RS422/485 line interfaces provide additional communication paths, supporting up to 230 Kbaud on RS232 and 3 Mbaud on RS422/485. Both UARTs feature 16-byte Fifos. UART 0 also provides RTS/CTS auto-flow-control. Data transfers can be accomplished by CPU (polling or interrupts) and DMA. The DModule2.BIOS provides configuration and data transfer functions.

Note: UART 0 (RS232) and the DSP 64-bit Timer share pins and cannot be used simultaneously. Internal use of this timer is not affected. Quadrature Decoder 0 and the UART0 handshake lines (RTS, CTS) share pins and cannot be used simultaneously.

I²C

The I²C interface can be used to control and configure peripherals like Audio Codecs, Image Sensors, and the analog front-ends of data acquisition boards. It is also usable to expand the system with additional GPIO signals and attach slow peripherals like temperature sensors. Data rates up to 400kBit/s and 7- and 10-bit addressing modes are supported.

Note: I²C and SPI share processor pins and cannot be used simultaneously. A SW-controlled multiplexer on the D.Module2 switches between functions.

SPI

The SPI interface can be used for peripheral expansions and as a communication path to micro-controllers. 8 and 16-bit transfers are supported, Master, Slave, and 4- and 5-wire configurations. The maximum clock rate is 50 MHz.

Note: SPI and I²C share processor pins and cannot be used simultaneously. A SW-controlled multiplexer on the D.Module2 switches between functions.

PRGIO

Most unused peripheral signals can be configured as GPIO pins. Additionally the D.Module2 adds another dedicated 16 bit pin-programmable I/O port.

PWM

The 6747 features a 3-channel enhanced PWM controller with 6 single edge, 6 symmetrical dual edge, or 3 asymmetrical dual edge outputs. The time-base is 16 bits. Additional features are dead-band generation, PWM chopping, and trip zone input. The Capture module, if not used, provides three additional auxiliary PWM outputs.

Note: PWM outputs 0A and 0B share pins with McASP1 and cannot be used simultaneously.

CAPTURE / COMPARE

Three 32-bit timers supporting single-shot capture of up to four event timestamps. Alternatively configurable as three auxiliary PWM outputs.

Note: Capture timer and McASP0 share pins and cannot be used simultaneously.

MCASP SERIAL PORTS

These two ports (McASP0 and McASP1) are use to serially connect A/D and D/A converters. Data rates up to 50 MBit/sec are supported for all common data formats (I²S, TDM, etc). McASP2 is not available on the D.Module2.

Note: Capture timer and McASP0 share pins and cannot be used simultaneously. PWM outputs 0A and 0B share pins with McASP 1 and cannot be used simultaneously.

QUADRATURE DECODER INTERFACE

Two channels can be used to interface rotary and linear encoders.

Note: Quadrature decoder 0 and the UART0 handshake lines (RTS, CTS) share pins and cannot be used simultaneously.

POWER SUPPLY

The D.Module2.C6747 operates from a 3.3V single supply. All other required voltages (core voltage, RS232 driver supply, USB VBUS host supply, etc.) are generated onboard by high-efficiency switch-mode converters and charge-pumps. The power supply is controlled by a supervisor chip, which guarantees a proper hardware reset on power-on, power-off, and brown-out conditions.

WATCHDOG

Stand-alone systems typically require methods for automatic recovery from system faults. One of these methods is activating the watchdog circuit. It will reset and reboot the system if the DSP program crashes and fails to trigger the

watchdog periodically. The watchdog can be enabled (but not disabled) by software, or permanently by closing a solder link.

RTC

The TMS320C6747 provides a real-time-clock which operates independent of the DSP power. The D.Module.C6747 provides mounting pads for a Panasonic EEC-EN0F204A 0.2F 2.5V Capacitor to buffer short-time power loss. Long-time power loss can be buffered by connecting an external 1.8V battery.

BOARD CONFIGURATION

D.Module2 boards use a jumperless design, all board settings are software-configurable in the Board Configuration Register. The configuration can be set by the user program, or – preferably – stored in the Module Configuration File. At system start-up the Module configuration File is read and DSP clock, bus clock, and other options are configured accordingly.

The Board Configuration Register also provides multiplexers to route external interrupt events and GPIO to the DSP, and control and status registers for all on-board peripherals.

D.MODULE2.BIOS

The BIOS is a set of API functions, permanently stored in the Flash Memory. These functions are copied to SDRAM at system start-up and are available to all user programs. BIOS functions cover initialization, configuration, and data transfer functions for the on-board peripherals. The reason to store these functions permanently in the Flash Memory, rather than providing them as a library, is the close coupling between low-level API functions and hardware: Should one of the module's peripherals need to be substituted during product lifetime, the BIOS will be adapted to the new hardware and the application program will continue to work without any changes.

USB functions

- open, close
- configure endpoints
- status change callback
- custom string descriptor table
- interrupt handler
- blockwrite, blockread
- low-level functions for user-defined interfaces

UART functions

- open, close
- configure
- write, blockwrite, write string
- read, blockread, read string

Flash Memory Functions

- open, get architecture information
- sector erase (64K bytes)
- subsector erase (4K bytes)
- write, write block
- read, read block
- write Intel-Hex file

Board Functions

- initialize
- bootload arbitrary program from Flash Memory
- get hardware and software revision
- DSP configuration and clocking
- external bus configuration
- delay
- watchdog enable and trigger
- interrupt and GPIO mapping
- peripheral configuration

SETUP AND RECOVERY PROGRAM

Also permanently stored in the Flash Memory are the Setup and Recovery utility programs. The Setup program communicates via RS232 or USB. It allows to upload Intel-Hex program and data files to the Flash Memory, upload a Module Configuration File, load and execute programs from Flash, and provides some basic debugging functions like reading and writing memory and memory-mapped peripherals. Setup is intended for field maintenance: Service technicians can upload program updates without direct access to the DSP hardware, and execute diagnostics and calibration programs stored in the Flash Memory.

The Recovery utility is stored in a hardware write protected Flash sector. Should the Flash be erased or overwritten accidentally, this program can be used to re-install the corrupted programs. Recovery uses a RS232 connection, even severe problems can be fixed in-field without special emulator programming equipment.

Setup is invoked during a module reset by pulling the SETUP_N input low, or at any time from within an application program by calling the BIOS bootload function: DM2_bootload (0x8000). Recovery is invoked at module reset by pulling both SETUP_N and IN0_N inputs low.

Peripheral Matrix

Due to pin-multiplexing on the TMS320C6747, not all peripherals can be used simultaneously. The following matrix shows these restrictions. Within a row, you can select one of the available functions. To change a pin configuration, the corresponding PINMUX register in the TMS320C6747 must be re-programmed.

Bold items	the default configuration (factory setting) of the D.Module2.C6747
normal items	alternative configuration
grayed italic items	function not available on the D.Module2.C6747

UART0 RxD, TxD	TM64P0_IN12,OUT12	*I2C0 SDA, SCL*	GP5[8,9]
UART0 RTS, CTS	**EQEP0 A, B**	SPI0 ENA, SCS	GP5[3,4]
	EQEP0 I, S	SPI0 SOMI, SIMO	GP5[0,1]
	EQEP1 I	SPI0 CLK	GP5[2]
	EQEP1 S	**SPI1 CLK**	GP5[7]
UART2 RxD, TxD		**SPI1 ENA, SCS**	GP5[12,13]
I2C1 SCL, SDA		**SPI1 SOMI, SIMO**	GP5[5,6]
McASP 1 AXR1 [3,4]	**EQEP1 A, B**		GP4[3,4]
McASP 1 AXR[1,0]			GP4[1,0]
McASP 1 AXR[9,2]			GP4[9,2]
McASP 1 AHCLKR			GP4[11]
McASP 1 ACLKR	ECAP2/APWM2		GP4[12]
McASP 1 AFSR			GP4[13]
McASP 1 AHCLKX		EPWM0 B	GP3[14]
McASP 1 ACLKX		EPWM0 A	GP3[15]
McASP 1 AFSX		EPWM SYNCI/O	GP4[10]
McASP 1 AXR[8,7]		**EPWM1 A,B**	GP4[8,7]
McASP 1 AXR[6,5]		**EPWM2 A,B**	GP4[6,5]
McASP 1 AMUTE		**EHRPWMTZ**	GP4[14]
McASP 1 AXR[11.10]			**GP[11, 10]**
McASP 0 ACLKR	ECAP1/APWM1		GP2[15]
McASP 0 AFSR			GP3[12]
McASP 0 AHCLKX			GP2[11]
McASP 0 ACLKX	ECAP0/APWM0		GP2[12]
McASP 0 AFSX			GP2[13]
McASP 0 AXR[14,15]			GP2[8,9]
McASP 0 AXR[11]			GP3[11]
McASP 0 AMUTE			

McASP 0 AXR[7, 8]	**MDIO CLK, D**		*GP3[7,8]*
McASP 0 AXR[0..6]	**RMII Data and Ctrl**		*GP3[0..6]*
McASP 0 AHCLKR	**RMII_MHZ_50**		*GP2[14]*
McASP 0 AXR[9,10]		**UART1 RxD, TxD**	*GP3[9,10]*
McASP 0 AXR[13,14]	**EMIFA OE, WE**		*GP2[7,3]*
MMCSD CLK, CMD	**EMIFA A1, A2**		*GP1[1,2]*
MMCSD DAT[0..3]	**EMIFA D[0..3]**		*GP0[0..3]*
MMCSD DAT[4..7]	**EMIFA D[4..7]**		*GP0[4..7]*
	EMIFA D[8..15]		*GP0[8..15]*
	EMIFA A[3..12]		*GP1[3..12]*
	EMIFA BA[0, 1]		*GP1[14,13]*
	EMIFA CS[2..5]		*GP2[5,6,1,2]*
	EMIFA WAIT		*GP2[10]*
	EMIFB (SDRAM)		*GP3[13], GP5[14,15], GP6[0..15], GP7[0..13],*

The following peripherals, not mentioned in the table above, are not avaialble on the D.Module.C6747:

- I2C0 (I²C Controller 0)
- UHPI (Host Port Interface)
- LCD (LCD Controller)
- McASP2 (Multi-Channel Audio Serial Port 2)
- AXR0[0..10, 13, 14], AHCLKR0 (McASP0 Signals)
- AXR1[10,11] (McASP1 Signals)
- MMCSD DAT[4..7] (MMC/SD 8-bit mode)

SPECIFICATIONS

DSP	Texas Instruments TMS320C6747, native 32/64-bit floating-point and 8/16/32-bit fixed support up to 2400 million instructions / 1800 floating point operations per second optional OMAP-L137 with additional 300 MHz ARM9 core
Memory	DSP-internal 32K Bytes level-1 data cache, 32K Bytes level-1 program cache 256K Bytes DSP-internal direct mapped or level-2 cache 128K Bytes DSP-internal shared RAM 64M Bytes SDRAM, operating at up to 133 MHz, 32 bits wide, 512M Byte/sec throughput 8M Bytes non-volatile Flash Memory, sector architecture , serial optional 2G Bytes NAND-Flash, 8 bit wide further non-volatile memory expansion via SD/MMC card interface
USB	USB 1.1 OHCI host controller, 12 MBit/sec USB 2.0 OTG controller , up to 480 MBit/sec
UART	UART 0: RS232 line interface, max. 230.4 Kbaud , 16 byte FIFO, RTS/CTS Auto-flow-control UART 1: RS422/485 line interface, max. 3 Mbaud , 16 byte FIFO
Ethernet	Two-port manageable switch and PHY, 100Base-Tx and 10Base-T, on-board magnetics for Port 0, external magnetics or Fiber Transceiver for Port 1
I²C	up to 400 Kbits/sec, master or slave operation, 7 and 10 bit addresses
SPI	supports up to 50 Mbits/sec, configurable as master or slave, 4- or 5- wire mode
Timer	built-in in DSP 64-bit timer, internal clocking 16-bit timer, internal or external clocking
Capture/Compare	3 Inputs, 32-bit single-shot capture of up to 4 event time stamps alternatively 3 auxiliary PWM outputs
PWM	3 high-resolution PWM controllers, 6 single-edge, 6 symmetric dual-edge, or 3 asymmetric dual edge outputs, dead-band generation, PWM chopping, and trip zone input
Quadrature Decoder	2 Channels
GPIO	16-bit dedicated GPIO port, bit-programmable most unused peripheral signals can be programmed as GPIO
External Bus Interface	16/32 bit wide data bus asynchronous operation two pre-decoded select signals with individually programmable timing external wait state request input up to 50M Bytes/sec throughput 3 interrupt inputs, also configurable as DMA trigger, 4 GPIO signals
Sync. Serial Ports	2 McASPs, independent receive and transmit channels, TDM, and I²S mode data rate up to 50 Mbit/sec
Real Time Clock	independent power supply rail
Watchdog	enabled by software or hardware, timeout: 1 second
Supply Voltage VCC	3.3 V ± 5%
Power Consumption	750mA typical
Operating Temperature	0 .. +70 °C
Logic Levels	LVTTL, High-Level min. 2V, max. 3.5V, Low Level min. -0.2V, max. 0.8V output drive: external bus interface: ± 24mA, all others ± 8mA
Size	86.8 x 58.4 mm, overall height: 19.5mm (can be reduced to 15.4 mm if JTAG connector is removed)
Weight	36g
Connectors	COM, EXP, BUS1 and BUS2 : Molex 71436-2164, mating connectors: Molex 71439-x164 Emulator: standard 14-pin header

TIMINGS

external bus asynchronous read

Timing	min	max	Description
t_{DATA_SETUP}	3ns		Data valid before RD_N rising edge
t_{DATA_HOLD}	0.5ns		Data hold after RD_N rising edge
t_{SETUP}	10ns	160ns	Setup Time Address and Chip Select Lines valid before RD_N falling edge, programmable in EMIFA Control Registers
t_{STROBE}	10ns	640ns	Strobe Time, nRD falling edge to RD_N rising edge programmable in EMIFA Control Registers
t_{HOLD}	10ns	70ns	Hold Time Address and Chip Select Lines valid after RD_N rising edge programmable in EMIFA Control Registers
t_{WAIT_SETUP}	46ns		WAIT_N setup to RD_N rising edge
t_W	20ns		external WAIT_N assertion width

external bus asynchronous write

Timing	min	max	Description
t_{DATA_SETUP}	= t_{SETUP}		Data valid before WR_N rising edge
t_{DATA_HOLD}	= t_{HOLD}		Data hold after WR_N rising edge
t_{SETUP}	10ns	160ns	Setup Time Address and Chip Select Lines valid before WR_N falling edge, programmable in EMIFA Control Registers
t_{STROBE}	10ns	640ns	Strobe Time, WR_N falling edge to WR_N rising edge programmable in EMIFA Control Registers
t_{HOLD}	10ns	70ns	Hold Time Address and Chip Select Lines valid after WR_N rising edge programmable in EMIFA Control Registers
t_{WAIT_SETUP}	46ns		WAIT_N setup to WR_N rising edge
t_W	20ns		external WAIT_N assertion width

Peripheral Timings

please refer to the TMS320C6747 data sheet and peripheral User's Guides.

MEMORY MAP

Address	Location	Width	Description
0x01C0.0000 .. 0x01C0.87FF	DSP		EDMA3 Controller
0x01C1.0000 .. 0x01C1.0FFF	DSP		Power Sleep Controller PSC0
0x01C1.1000 .. 0x01C1.1FFF	DSP		PLL
0x01C1.4000 .. 0x01C1.4FFF	DSP		SYSCFG
0x01C2.0000 .. 0x01C2.0FFF	DSP		Timer64P0
0x01C2.1000 .. 0x01C2.1FFF	DSP		Timer64P1
0x01C2.2000 .. 0x01C2.2FFF	DSP		I²C0 (not available on D.Module2.C6747)
0x01C2.3000 .. 0x01C2.3FFF	DSP		RTC
0x01C4.0000 .. 0x01C4.0FFF	DSP		MMC/SD Controller
0x01C4.1000 .. 0x01C4.1FFF	DSP		SPI0
0x01C4.2000 .. 0x01C4.2FFF	DSP		UART0
0x01D0.0000 .. 0x01D0.2FFF	DSP		McASP0
0x01D0.4000 .. 0x01D07FFF	DSP		McASP1
0x01D0.8000 .. 0x01D0.AFFF	DSP		McASP2 (not available on D.Module2.C6747)
0x01D0.C000 .. 0x01D0.CFFF	DSP		UART1
0x0x1D.D000 .. 0x01D0.DFFF	DSP		UART2 (not available on D.Module2.C6747)
0x01E0.0000 .. 0x01E0.FFFF	DSP		USB0
0x01E1.0000 .. 0x01E1.0FFF	DSP		UHPI (not available on D.Module2.C6747)
0x01E1.2000 .. 0x01E1.2FFF	DSP		SPI1
0x01E1.3000 .. 0x01E1.3FFF	DSP		LCD Controller (not available on D.Module2.C6747)
0x01E2.0000 .. 0x01E2.4FFF	DSP		EMAC and MDIO
0x01E2.5000 .. 0x01E2.5FFF	DSP		USB1
0x01E2.6000 .. 0x01E2.6FFF	DSP		GPIO
0x01E2.7000 .. 0x01E2.7FFF	DSP		Power-Sleep Controller PSC1
0x01E2.8000 .. 0x01E2.8FFF	DSP		I²C1
0x01F0.0000 .. 0x01F0.1FFF	DSP		High Resolution PWM HRPWM0
0x01F2.0000 .. 0x01F0.3FFF	DSP		High Resolution PWM HRPWM1
0x01F4.0000 .. 0x01F0.5FFF	DSP		High Resolution PWM HRPWM2
0x01F0.6000 .. 0x01F0.6FFF	DSP		Capture Module ECAP 0
0x01F0.7000 .. 0x01F0.7FFF	DSP		Capture Module ECAP 1
0x01F0.7000 .. 0x01F0.8FFF	DSP		Capture Module ECAP 2
0x01F0.9000 .. 0x01F0.9FFF	DSP		Quadrature Decoder EQEP0
0x01F0.A000 .. 0x01F0.AFFF	DSP		Quadrature Decoder EQEP1
0x1170.0000 .. 0x117F.FFFF	DSP	256 bit	ROM
0x1180.0000 .. 0x1183.FFFF	DSP	256 bit	L2RAM / L2 Cache
0x11E0.0000 .. 0x11E0.7FFF	DSP	256 bit	L1PRAM / L1P Cache
0x11F0.0000 .. 0x11F0.7FFF	DSP	256 bit	L1DRAM / L1D Cache
0x4000.0000 .. 0x5FFF.FFFF	EMIFA	16 bit	EMIFA SDRAM (not available on D.Module2.C6747)
0x6000.0000 .. 0x61FF.FFFF	EMIFA	8 bit	optional NAND Flash
0x6200.0000 .. 0x6200.003D	EMIFA	8/16 bit	Board Configuration Registers
0x6400.0000 .. 0x6400.3FFF	EMIFA	16/32 bit	ext. Bus Interface CS0
0x6600.0000 .. 0x6600.3FFF	EMIFA	16/32 bit	ext. Bus Interface CS1
0x6800.0000 .. 0x6800.7FFF	DSP		EMIFA Controller
0x8000.0000 .. 0x8001.FFFF	DSP		Shared RAM
0xB000.0000 .. 0xB000.7FFF	DSP		EMIFB Controller
0xC000.0000 .. 0xC3FF.FFFF	EMIFB	32 bit	EMIFB SDRAM

BOARD CONFIGURATION REGISTERS

Register	D7	D6	D5	D4	D3	D2	D1	D0
USBCTRL	-	-	USB1 VBUS_OC	USB1 VBUS	-	USB0 VBUS_OC	USB0 VBUS	USB0 ID
UARTCTRL	-	-	-	-	-	-	DRVEN_1	DRVEN_0
BUSCTRL	RESOUT	-	-	-	-	16 HI/LO	CE1 16/32	CE0 16/32
WDOGCTRL	-	-	-	-	-	-	ENABLE	TRIGGER
DSPCTRL	RESET	MARKER	-	BOOT7	BOOT3	BOOT2	BOOT1	BOOT0
SETUPSTAT	-	-	-	-	-	SETUP	IN1	IN0
FLASHCTRL	-	-	-	-	-	-	SER_WP	NAND_WP
INTMUXLO	GP5[10]_INT_SOURCE				GP2[0]_INT_SOURCE			
GPIOMUXLO	GPIO1				GPIO0			
GPIOMUXHI	GPIO3				GPIO2			
ETHCTRL	PHYRES	-	-		-	-	PHY2_BIAS	-
EXPMUX				EMIFA / SDMMC	UART0 / TMR64	UART0HS/ EQEP0	SPI / I²C Select	

Register	D15:D0
PRGIO_DAT	read: PRGIO[15:0] input, write: PRGIO[15:0] output
PRGIO_DIR	Direction of PRGIO[15:0]: 0 = input, 1 = output
TMR16_CTRL	Timer Control
TMR16_PRD	Timer Period
TMR16_CNT	Timer Counter

USBCTRL:

D5	USB1 VBUS_OC	read only	overcurrent on USB1 VBUS line
D4	USB1 VBUS	read/write	turn on USB1 VBUS
D2	USB0 VBUS_OC	read only	overcurrent on USB1 VBUS line
D1	USB0 VBUS	read only	USB0 VBUS on (USB0 VBUS is controlled via DSP)
D0	USB0 ID	read/write	USB0 ID (used for OTG mode)

UARTCTRL:

D1	DRVEN1	read/write	UART1 RS422/485 driver enable
D0	DRVEN0	read/write	UART0 RS422/485 driver enable

BUSCTRL:

D7	RESEOUT	read/write	assert RESOUT_N on ext. Bus Interface
D2	16 HI/LO	read/write	select D[31:16] or D[15:0] for 16-bit transfers
D1	CE1 16/32	read/write	select 16 or 32-bit transfers for CE1 memory range
D0	CE0 16/32	read/write	select 16 or 32-bit transfers for CE0 memory range

WDOGCTRL:

D1	ENABLE	write once	Watchdog Enable
D0	TRIGGER	write only	Watchdog Trigger (writing a '1' triggers the watchdog timer)

DSPCTRL:

D7	RESET	write once	reset DSP
D6	MARKER	read/write	marker bit, uneffected by a DSP reset, only reset by power-off
D[4:0]	BOOT[7,3:0]	read/write	DSP bootloader configuration

SETUPSTAT:

D2	SETUP	read only	state of SETUP_N pin
D1	IN1	read only	state of IN1_N pin
D0	IN0	read only	state of IN0_N pin

FLASHCTRL:

D1	SER_WP	write once	assert serial Flash Write Protection
D0	NAND_WP	write onlce	assert NAND Flash Write Protection

INTMUXLO:

D[7:4]	GP5[10]_INT_SRC	read/write	interrupt source for GP5[10]
D[3::0]	GP4[0]_INT_SRC	read/write	interrupt source for GP4[0]

valid settings:

0000	none
0001	ext. Bus nINT0
0010	ext. Bus nINT1
0011	ext. Bus nINT2
0100	USB0 VBUS Overcurrent
0101	USB1 VBUS Overcurrent
0110	Timer16

GPIOMUXLO:

D[7:4]	GPIO1 routing	read/write	source/destination for ext. Bus GPIO1
D[3:0]	DPIO0 routing	read/write	source/destination for ext. Bus GPIO0

GPIOMUXHI:

D[7:4]	GPIO3 routing	read/write	source/destination for ext. Bus GPIO3
D[3:0]	DPIO2 routing	read/write	source/destination for ext. Bus GPIO2

valid settings for GPIOMUX:

0000	GPIOx is input, routed to DSP GP5[11] rsp. GP2[4]
0001	GPIOx is input, routed to DSP Timer 64P0_IN12
0011	GPIOx is input, routed to Timer 16 input
1000	GPIOx is output, driven from DSP GP5[11] rsp GP2[4]
1001	GPIOx is output, driven from DSP Timer 64P0_OUT12
1011	GPIOx is output, driven from Timer16 output
1110	GPIOx is output, logic 0
1111	GPIOx is output, logic 1

GPIO0 and GPIO2 can use DSP signal GP2[4], GPIO1 and GPIO3 can use DSP signal GP5[11]

ETHCTRL:

D7	PHYRES	read/write	reset PHY
D2	PHY2BIAS	read/write	provide BIAS for PHY2 receiver (in Fiber mode)

EXPMUX

D4	EMIFA/SDMMC	read/write	select EMIFA or SDMMC interface
D3	UART0/TMR64	read/write	select UART0 or DSP Timer TM64P0_12
D2	UART0HS/EQEP0	read/write	select UART0 handshake (RTS/CTS) or EQEP0
D[1:0]	SPI/I2C	read/write	00 – SPI Flash 01 – SPI PHY 10 – SPI External 11 – I²C

PINOUT AND SIGNAL DESCRIPTION

COM Connector

Signal	Pin	Type	Description
GND_IN	1,2,3,4	PWR	Power Supply Input, 0V
VCC_IN	5,6,7,8	PWR	Power Supply Input, 3.3V
SETUP_N	9	I	Setup Input, active low, internal 10K pull-up, start Setup-Utility if found low at reset
IN0_N	10	I	active low, internal 10K pull-up, start Recovery-Utility if SETUP_N and IN0_N are found low at reset
IN1_N	12	I	active low, internal 10K pull-up, reserved for configuration
RESIN_N	11	I	Reset Input, active low, internal 10K pull-up
USB0_VCC	13	I	USB 0 Power, supplied by Host or Hub, used to detect USB cable
USB0_GND	15	I	USB 0 power and reference signal ground
USB0_DP	14	IO	USB 0 data, non-inverted signal
USB0_DM	16	IO	USB 0 data, inverted signal
CTS0	19	I	UART0, RS232 CTS
RTS0	20	O	UART0, RS232 RTS
RXD0	21	I	UART0, RS232 data input
TXD0	22	O	UART0, RS232 data output
RXD1-	25	I	UART1, RS422 inverted data input
TXD1-	26	O	UART1, RS422 inverted data output
RXD1+	27	I	UART1, RS422 non-inverted data input
TXD1+	28	O	UART1, RS422 non-inverted data output
ETH0_GND	29, 30		Port 0 100Base-Tx Ethernet ground
ETH0_RX+	31	I	Port 0 100Base-Tx Ethernet non-inverted data input
ETH0_RX-	33	I	Port 0 100Base-Tx Ethernet inverted data input
ETH0_TX+	32	O	Port 0 100Base-Tx Ethernet non-inverted data output
ETH0_TX-	34	O	Port 0 100Base-Tx Ethernet inverted data output
SCL	37	IOZ	I²C Bus Clock, internal 4K7 pull-up
SDA	38	IOZ	I²C Bus Data, internal 4K7 pull-up
PRGIO 0..15	43,45,46,48, 49,50,51,53 54,56,57,58, 59,61,62,64	IOZ	programmable I/O signal from Board Logic
SGND	17,18,23,24, 35,36,40,41, 44,47,52,55, 60,63		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

EXP Connector

Signal	Pin	Type	Description
ETH1_TX+	2	O	Port 1 Ethernet non-inverted data output, connect to PHY or Fiber Transceiver
ETH1_TX-	4	O	Port 1 Ethernet inverted data output, connect to PHY or Fiber Transceiver
ETH1_RX+	8	I	Port 1 Ethernet non-inverted data input, connect to PHY or Fiber Transceiver
ETH1_RX-	10	I	Port 1 Ethernet inverted data input, connect to PHY or Fiber Transceiver
ETH1_LED1	3	O	Port 1 Ethernet Link LED, connect LED to 3.3V
ETH1_LED2	5	O	Port 1 Ethernet Activity LED, connect LED to 3.3V
ETH1_SD	7	I	Port 1 Ethernet Signal Detect input, connect to Fiber Transceiver
USB0_ID	12	I	USB 0 ID, connect to pin4 of a micro-AB connector for OTG
USB1_VBUS	16	O	USB1 Host VBUS output
USB1_DP	18	IO	USB1 data, non-inverted
USB1_DM	20	IO	USB1 data, inverted
MMCSD_CLK	11	O	MMC/SD Card Interface Clock
MMCSD_CMD	13	IO	MMC/SD Card Interface Command
MMCSD_DAT0	15	IO	MMC/SD Card Interface Data Bit 0
MMCSD_DAT1	19	IO	MMC/SD Card Interface Data Bit 1
MMCSD_DAT2	21	IO	MMC/SD Card Interface Data Bit 2
MMCSD_DAT3	23	IO	MMC/SD Card Interface Data Bit 3
EQEP0A	24	I	Quadrature Decoder 0, A channel
EQEP0B	26	I	Quadrature Decoder 0, B channel
EQEP0I	28	I	Quadrature Decoder 0, Index Pulse
EQEP0S	32	I	Quadrature Decoder 0, Strobe (optional)
EQEP1A	27	I	Quadrature Decoder 1, A channel
EQEP1B	29	I	Quadrature Decoder 1, B channel
EQEP1I	31	I	Quadrature Decoder 1, Index Pulse
EPWM0A	34	O	PWM Channel 0 output A
EPWM0B	36	O	PWM Channel 0 output B
EPWM1A	35	O	PWM Channel 1 output A
EPWM1B	37	O	PWM Channel 1 output B
EPWM2A	40	O	PWM Channel 2 output A
EPWM2B	42	O	PWM Channel 2 output B
EPWMSYNC	39	IO	PWM Sync Input or Output
EPWMTZ	44	I	PWM Trip Zone Input , also AMUTE1 (McASP1 Mute Output)
ECAP0/APWM0	43	IO	Capture Compare Channel 0 or Auxiliary PWM 0
ECAP1/APWM1	45	IO	Capture Compare Channel 1 or Auxiliary PWM 1
ECAP2/APWM2	47	IO	Capture Compare Channel 2 or Auxiliary PWM 2

SPI_SIMO	48	IO	SPI Slave In / Master Out Data
SPI_SOMI	50	IO	SPI Slave Out / Master In Data
SPI_CLK	52	IO	SPI Clock Master:Out, Slave: In
SPI_CS	56	IO	SPI Slave Select, Master: OUT, Slave: In
SPI_ENA	53	IO	SPI Enable
RTCVDD	51	PWR	1.8V external supply for long-time RTC buffering
AXR1[9]	55	IO	additional McASP1 Receive/Transmit Data Serializer
AXR1[2]	59	IO	additional McASP1 Receive/Transmit Data Serializer
AHCLKR1	61	I	McASP1 external Receive Master Clock
AHCLKX1	63	I	McASP1 external Transmit Master Clock
AMUTE0	58	O	McASP0 Mute Output
AXR0[11]	60	IO	additional McASP0 Receive/Transmit Data Serializer
AHCLKX0	64	I	McASP0 external Transmit Master Clock
SGND	1,6,9,14, 17,22,25,30, 33,38,41,46, 49,54,57,62		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

BUS 1 Connector

Signal	Pin	Type	Description
VCC_OUT	1, 2	PWR	Power Supply Output to Peripherals, +3.3V
GND_OUT	3, 4	PWR	Power Supply Output to Peripherals, 0V
AGND	59, 60	PWR	Analogue Power Supply to Peripherals, 0V, not connected
AVCC+	61, 62	PWR	Analogue Power Supply to Peripherals, positive voltage rail, not connected
AVCC-	63, 64	PWR	Analogue Power Supply to Peripherals, negative voltage rail, not connected
RESOUT_N	5	O	Reset Output to Peripherals, active low
BUSCLK	6	O	Bus Clock, use if external bus configured to synchronous operation
INT0_N, INT1_N, INT2_N	7, 9, 10	I	External Interrupt Inputs, active low, internal 1K pull-up
BE2_N, BE3_N	12, 14	O	reserved for Byte Enable, GND on D.Module2.C6747
OE_N	13	O	Output Enable, active low, asserted during Read Cycles = RD_N
RD_N	15	O	Read Strobe, active low
WR_N	17	O	Write Strobe, active low
WAIT_N	18	I	Wait State Request, active low, internal 1K pull-up
CS0_N	20	O	Chip Select 0, active low = DSP CS4
CS1_N	22	O	Chip Select 1, active low = DSP CS5
A0..A5	21,23,25,26, 28,29	O	Address Bus = DSP A0..A5
A16..A19	30,31,33,34	O	Address Bus, A16=DSP A10, A17=DSP A11, A18=DSP A12, A19=DSP BA0
D16..D31	36,37,38,39, 41,42,44,45, 46,47,49,50, 52,53,54,55	IOZ	Data Bus
GPIO0, GPIO1	57, 58	IOZ	General Purpose IO
SGND	8,11,16,19, 24,27,32,35, 40,43,48,51, 56		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

BUS 2 Connector

Signal	Pin	Type	Description
VCC_OUT	63, 64	PWR	Power Supply Output to Peripherals, +3.3V
GND_OUT	61, 62	PWR	Power Supply Output to Peripherals, 0V
AGND	5, 6	PWR	Analogue Power Supply to Peripherals, 0V, not connected
AVCC+	3, 4	PWR	Analogue Power Supply to Peripherals, positive voltage rail, not connected
AVCC-	1, 2	PWR	Analogue Power Supply to Peripherals, negative voltage rail, not connected
GPIO2, GPIO3	7, 8	IOZ	General Purpose IO
D0..D15	9,10,11,12, 14,15,16,17, 19,20,22,23, 24,25,27,28	IOZ	Data Bus
A6..A15	30,31,32,33, 35,36,38,39, 40,41	O	Address Bus, A6..A11 = DSP A6..A11, A12..A15 = GND
BE0_N, BE1_N	43, 44	O	reserved for Byte Enable, GND on D.Module2.C6747
DATR0	46	I	Synchronous Serial Port 0, data receiver
CLKR0	47	IO	Synchronous Serial Port 0, receiver clock input or output
FSR0	48	IO	Synchronous Serial Port 0, receiver frame sync input or output
DATX0	49	O	Synchronous Serial Port 0, data transmitter
CLKX0	51	IO	Synchronous Serial Port 0, transmitter clock input or output
FSX0	52	IO	Synchronous Serial Port 0, transmitter frame sync input or output
DATR1	54	I	Synchronous Serial Port 1, data receiver
CLKR1	55	IO	Synchronous Serial Port 1, receiver clock input or output
FSR1	56	IO	Synchronous Serial Port 1, receiver frame sync input or output
DATX1	57	O	Synchronous Serial Port 1, data transmitter
CLKX1	58	IO	Synchronous Serial Port 1, transmitter clock input or output
FSX1	59	IO	Synchronous Serial Port 1, transmitter frame sync input or output
RESOUT_N	60	O	Reset Output to Peripherals, active low
SGND	13,18,21,26, 29,34,37,42, 45,50,53,		Signal Ground (signal current return path)

I – Input, O – Output, IO – bidirectional, Z – high impedance, PWR – power

BUS 1

Pin	Signal	Signal	Pin
1	VCC_OUT	VCC_OUT	2
3	GND_OUT	GND_OUT	4
5	RESOUT_N	BUSCLK	6
7	INT0_N	SGND	8
9	INT1_N	INT2_N	10
11	SGND	BE2_N	12
13	OE_N	BE3_N	14
15	RD_N	SGND	16
17	WR_N	WAIT_N	18
19	SGND	CS0_N	20
21	A0	CS1_N	22
23	A1	SGND	24
25	A2	A3	26
27	SGND	A4	28
29	A5	A16	30
31	A17	SGND	32
33	A18	A19	34
35	SGND	D16	36
37	D17	D18	38
39	D19	SGND	40
41	D20	D21	42
43	SGND	D22	44
45	D23	D24	46
47	D25	SGND	48
49	D26	D27	50
51	SGND	D28	52
53	D29	D30	54
55	D31	SGND	56
57	GPIO0	GPIO1	58
59	AGND	AGND	60
61	AVCC+	AVCC+	62
63	AVCC-	AVCC-	64

COM

Pin	Signal	Signal	Pin
1	GND_IN	GND_IN	2
3	GND_IN	GND_IN	4
5	VCC_IN	VCC_IN	6
7	VCC_IN	VCC_IN	8
9	SETUP_N	IN0_N	10
11	RESIN_N	IN1_N	12
13	USB0_VBUS	USB0_DP	14
15	USB0_GND	USB0_DM	16
17	SGND	SGND	18
19	CTS_0	RTS_0	20
21	RXD_0	TXD_0	22
23	SGND	SGND	24
25	RXD_1-	TXD_1-	26
27	RXD_1+	TXD_1+	28
29	ETH0_GND	ETH0_GND	30
31	ETH0_RX+	ETH0_TX+	32
33	ETH0_RX-	ETH0_TX-	34
35	SGND	SGND	36
37	SCL	SDA	38
39	rsvd	SGND	40
41	SGND	rsvd (CLKIN)	42
43	PRGIO0	SGND	44
45	PRGIO1	PRGIO2	46
47	SGND	PRGIO3	48
49	PRGIO4	PRGIO5	50
51	PRGIO6	SGND	52
53	PRGIO7	PRGIO8	54
55	SGND	PRGIO9	56
57	PRGIO10	PRGIO11	58
59	PRGIO12	SGND	60
61	PRGIO13	PRGIO14	62
63	SGND	PRGIO15	64

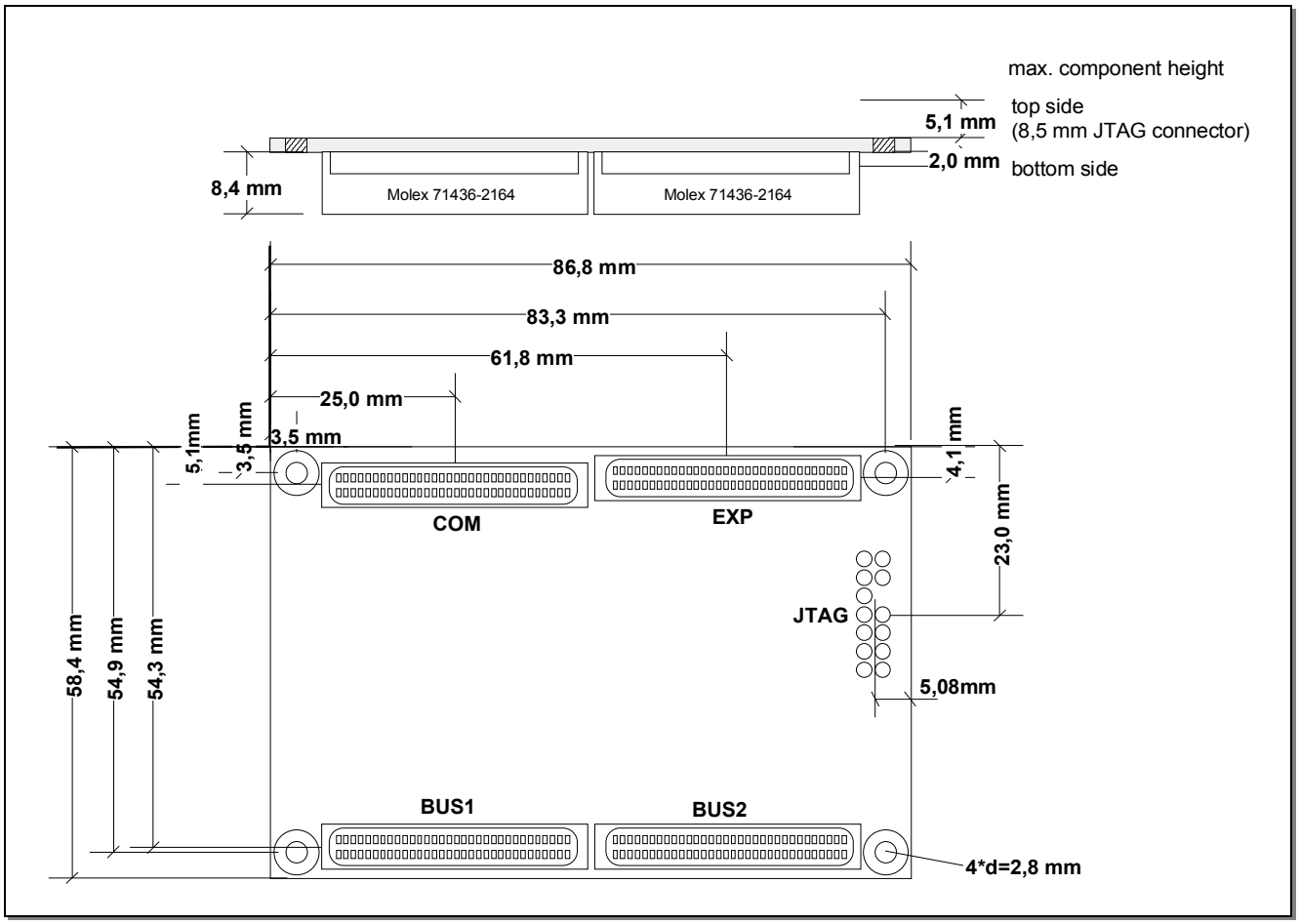
BUS 2

Pin	Signal	Signal	Pin
1	AVCC-	AVCC-	2
3	AVCC+	AVCC+	4
5	AGND	AGND	6
7	GPIO2	GPIO3	8
9	D0	D1	10
11	D2	D3	12
13	SGND	D4	14
15	D5	D6	16
17	D7	SGND	18
19	D8	D9	20
21	SGND	D10	22
23	D11	D12	24
25	D13	SGND	26
27	D14	D15	28
29	SGND	A6	30
31	A7	A8	32
33	A9	SGND	34
35	A10	A11	36
37	SGND	A12	38
39	A13	A14	40
41	A15	SGND	42
43	BE0_N	BE1_N	44
45	SGND	DATR0	46
47	CLKR0	FSR0	48
49	DATX0	SGND	50
51	CLKX0	FSX0	52
53	SGND	DATR1	54
55	CLKR1	FSR1	56
57	DATX1	CLKX1	58
59	FSX1	RESOUT_N	60
61	GND_OUT	GND_OUT	62
63	VCC_OUT	VCC_OUT	64

EXP

Pin	Signal	Signal	Pin
1	SGND	ETH1_TX+	2
3	ETH1_LED1	ETH1_TX-	4
5	ETH1_LED2	SGND	6
7	ETH1_SD	ETH1_RX+	8
9	SGND	ETH1_RX-	10
11	MMCSD_CLK	USB0_ID	12
13	MMCSD_CMD	SGND	14
15	MMCSD_DAT0	USB1_VBUS	16
17	SGND	USB1_DP	18
19	MMCSD_DAT1	USB1_DM	20
21	MMCSD_DAT2	SGND	22
23	MMCSD_DAT3	EQEP0A	24
25	SGND	EQEP0B	26
27	EQEP1A	EQEP0I	28
29	EQEP1B	SGND	30
31	EQEP1I	EQEP0S	32
33	SGND	EPWM0A	34
35	EPWM1A	EPWM0B	36
37	EPWM1B	SGND	38
39	EPWMSYNC	EPWM2A	40
41	SGND	EPWM2B	42
43	ECAP/APWM 0	EPWMTZ	44
45	ECAP/APWM 1	SGND	46
47	ECAP/APWM 2	SPI_SIMO	48
49	SGND	SPI_SOMI	50
51	RTCVDD	SPI_CLK	52
53	SPI1_ENA	SGND	54
55	AXR1[9]	SPI_CS	56
57	SGND	AMUTE0	58
59	AXR1[2]	AXR0[11]	60
61	AHCLKR1	SGND	62
63	AHCLKX1	AHCLKX0	64

MECHANICAL DIMENSIONS



ORDERING INFORMATION

D.Module2.C6747	standard module
Options	on request: 2 G Bytes NAND Flash, OMAP-L137 processor, industrial temperature grade please contact D.SignT for availability and minimum order quantities
DS.6747	Development Support Base Package including support software, base board, cables, power supply, and documentation
TMDSCCSALL-1	Code Generation Tools, Debugger, IDE
XDS560R	High Performance USB2.0 JTAG in-circuit Emulator
XDS510_PLUS	USB2.0 JTAG in-circuit Emulator
XDS510 galvanic	galvanic isolated JTAG in-circuit emulator

Additional Options On Volume Purchase

For volume purchase D.SignT offers customer specific modifications of the hardware either to reduce costs through reduced functionality or to increase functionality to meet the customers application requirements. Extensive experience in custom designs and the powerful engineering tools of our development department bring your application and our DSP know how together for your solution. Please contact D.SignT directly.

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Availability

Our standard D.Modules are available typically ex-stock.- For special modifications or non-standard D.Module2 please consult our sales department.

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