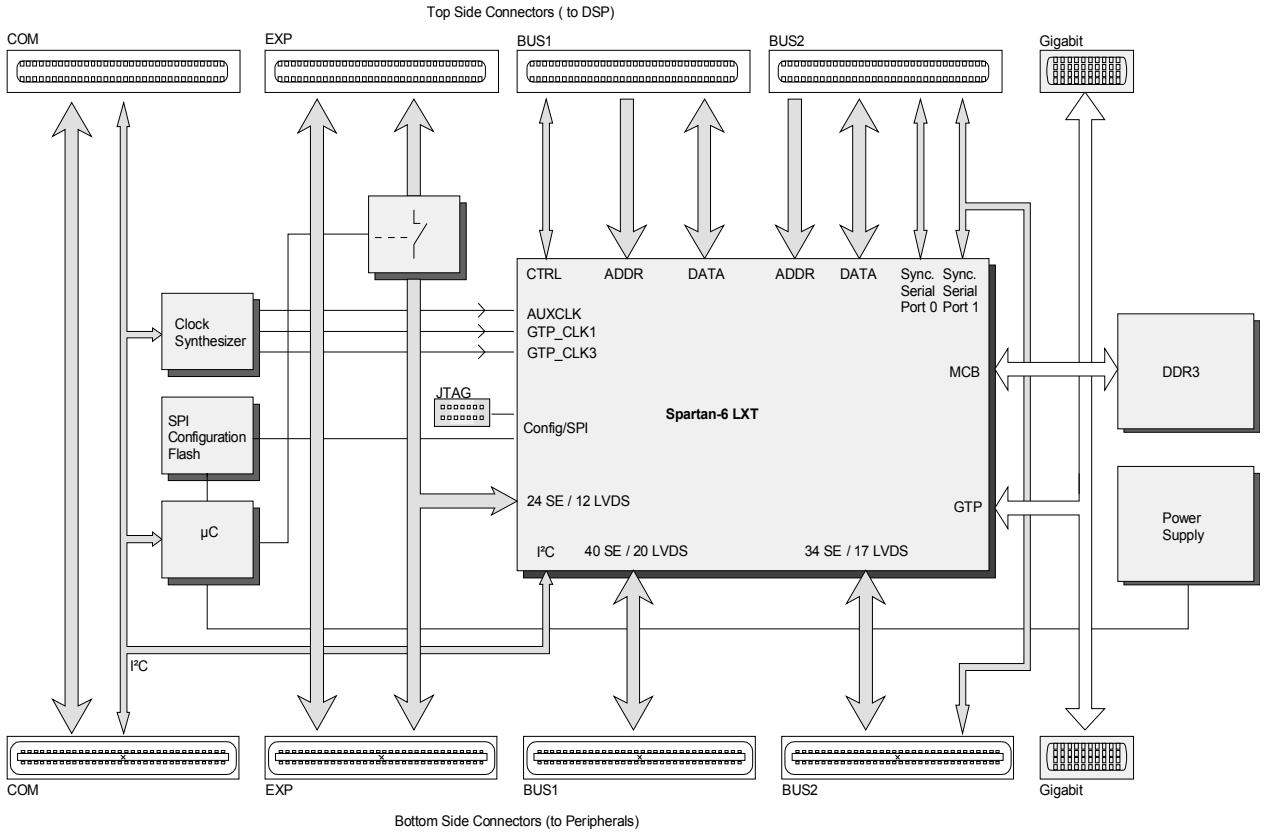
D.Module2.6SLX45T Technical Data Sheet

Board Revision 1.0 **Document Rev. 1.0** **Nov/2014**

SUMMARY

- **Xilinx Spartan6 XC6SLX45T FPGA (optional LX100T)**
- **DSP Interface:**
  - **32-bit D.Module2 Bus Interface**
  - **One Gigabit Transceiver (SRIO)**
  - **Two Synchronous Serial Ports**
  - **I²C**
  - **D.Module2 Expansion Port with 12 LVDS-pairs / 24 single-ended signals**
  - **access to the FPGA Configuration Flash for in-system updates**
- **User-I/O:**
  - **up to 49 LVDS-pairs / 98 single-ended signals**
  - **programmable I/O voltage 1.8, 2.5, or 3.3V**
  - **3 Gigabit Transceivers (PCI/e, JESD204/A, SGMII, SATA, SRIO)**
  - **FMC LPC signal standard compatible**
- **128M bytes local DDR3 memory**
- **3.3V single-supply**



The D.Module2.6SLX45T offers high-speed data preprocessing and connectivity for D.Module2 DSP boards.

The split D.Module2 bus interface on top and bottom-side connectors BUS1 and BUS2 allows to insert the FPGA board between the DSP and a data acquisition board, or operation of the FPGA in parallel with other D.Module2 peripheral boards. The signals on the bottom connectors are compatible to the industry standard ANSIVITA 57.1 FMC (LPC), providing a glueless connection to a wide variety of off-the-shelf high-speed data acquisition and interface cards. A Eurocard sized evaluation board with FMC and D.Module2 carrier sites is available for rapid prototyping.

The expansion interface (EXP) is optimized for image processing and video interfaces: it can accommodate two HDMI ports or a Camera Link Base interface. Alternatively It can be used as a data link to the DSP.

The Spartan 6LXT FPGA family is perfectly suited for high-speed serial communication: Four Gigabit Transceiver Ports are available for PCI/e, SATA, SGMII, or SRIO links, or used as high speed data converter interfaces using the JESD204(A) standard. One Gigabit transceiver is routed to the DSP (top-side) connector, three are available on the bottom side connector.

The FPGA DSP-slices efficiently handle data preprocessing tasks like filters, convolutions and transformations. A dedicated memory controller provides the interface to 128M bytes DDR3 RAM for local storage.

A micro controller on the FPGA board provides DSP access to the FPGA configuration memory for in-system updates. Additionally it monitors the power supply rails, allows access to the FPGA configuration pins, controls the Bank 0 and 2 I/O voltage, and the Expansion Bus switches.

During development the FPGA can be conveniently configured via JTAG.

FPGA

Xilinx Spartan-6 XC6SLX45T or XC6SLX100T

Resources	XC6SLX45T	XC6SLX100T
logic cells	43661	101261
flip flops	54576	126576
logic slices *1	6822	15822
DSP48A1 slices *2	58	180
clock manager *3	4	6
block RAM	2088k bit	4824k bit

*1) logic slice = four 6-input look-up tables, 8 flip-flops
*2) DSP48A1 slice = 18x18 mult, adder/accumulator
*3) clock manager = 2 DCM, 1PLL

configuration: SPI Flash and JTAG

MEMORY

DDR3-1066, 128M Bytes (64M x 16), integrated dedicated memory control block in FPGA.

8M Bytes SPI Configuration Flash

CLOCKS

Si5338 clock synthesizer, I²C programmable, generates AUXCLK and GTP reference clocks.

D.MODULE2 BUS INTERFACE (BUS1, BUS2)

32-bit data bus, 20 address lines, 10 control lines. Top and Bottom connectors are separately connected to the FPGA, facilitating insertion of the FPGA into the signal processing data flow. Asynchronous or Pipelined Synchronous Configuration is supported depending on the DSP board capabilities. Besides the parallel bus interface the FPGA is also connected to the two D.Module2 standard DSP synchronous serial ports, 3 interrupt inputs, and 4 GPIO signals

The FPGA signals connected to the BUS1 and BUS2 bottom side connectors are routed as differential pairs with matched trace length and are compatible with the ANSIVITA 57.1 FMC standard. The IO-Voltage of these signals is programmable as 1.8, 2.5 or 3.3V.

D.MODULE2 EXPANSION INTERFACE (EXP)

24 LVTTL / 12 LVDS signals, including four signals (2 LVDS) connected to global FPGA clock I/O pads. The top connector can be isolated from the DSP EXP connector to use these signals as User-I/O, e.g. 2x HDMI, 1x Camera Link Base, or GPIO. Alternatively, with the top-side connector connected to the DSP, these signals provide an alternative data path to the DSP board, e.g. via Tiger Sharc Link Ports.

GIGABIT TRANSCEIVER (GTP)

Four ports, each consisting of a transmitter, receiver, and a reference clock. Two external reference clock inputs, two programmable clocks on-board. Data rate up to 3.125 Gb/sec., integrated PCI/e endpoint. One transceiver is connected to the top side connector to be used as a SRIO interface to the DSP board, three transceivers are routed to the bottom side connector to be used as external interfaces. Supported standards are PCI/e, SRIO, JESD204(A), SATA and SGMII.

Two additional LVTTL signals are provided as GPIO.

I²C

An I²C interface is used as a communication path between the DSP board and a micro-controller on the FPGA board. This allows the DSP to (re-)program the FPGA configuration memory, control board configuration, and monitor supply voltages. The FPGA and the Si5338 clock synthesizer are also connected to the I²C bus.

ADDITIONAL SIGNALS

Two GPIO signals for debugging and two LEDs.

POWER SUPPLY

The D.Module2.6SLX45T operates from a 3.3V single supply. All other required voltages are generated on-board.. Power supply monitoring is provided via I2C. The IO voltage of the FPGA signals in bank 0 and 2 (signals on bottom side BUS1 and BUS2 connectors and the EXP connector) is programmable to accommodate various interface standards.

FPGA PIN ASSIGNMENTS

See spreadsheet dm2fpga6slxt.xls

CONNECTORS

BUS1, BUS2, COM, EXP top-side: Molex 71439-0164
BUS1, BUS2, COM, EXP bot-side: Molex 71436-2164
GBT top-side: Molex SEARAY 46557-1545
GBT bot-side: Molex SEARAY 46556-1145

OPERATING CONDITIONS

Temperature 0..70°C

Supply Voltage 3.3V +/-5% Current: TBD

BUS 1

Pin	Signal	Signal	Pin
1	VCC_OUT	VCC_OUT	2
3	GND_OUT	GND_OUT	4
5	RESOUT_N	BUSCLK *1	6
7	INT0_N *1	SGND	8
9	INT1_N *1	INT2_N *1	10
11	SGND	BE2_N *1	12
13	OE_N *1	BE3_N *1	14
15	RD_N *1	SGND	16
17	WR_N *1	WAIT_N *1	18
19	SGND	CS0_N *1	20
21	A0 *1	CS1_N *1	22
23	A1 *1	SGND	24
25	A2 *1	A3 *1	26
27	SGND	A4 *1	28
29	A5 *1	A16 *1	30
31	A17 *1	SGND	32
33	A18 *1	A19 *1	34
35	SGND	D16 *1	36
37	D17 *1	D18 *1	38
39	D19 *1	SGND	40
41	D20 *1	D21 *1	42
43	SGND	D22 *1	44
45	D23 *1	D24 *1	46
47	D25 *1	SGND	48
49	D26 *1	D27 *1	50
51	SGND	D28 *1	52
53	D29 *1	D30 *1	54
55	D31 *1	SGND	56
57	GPIO0 *1	GPIO1 *1	58
59	AGND	AGND	60
61	AVCC+	AVCC+	62
63	AVCC-	AVCC-	64

COM

Pin	Signal	Signal	Pin
1	GND_IN	GND_IN	2
3	GND_IN	GND_IN	4
5	VCC_IN	VCC_IN	6
7	VCC_IN	VCC_IN	8
9	SETUP_N	IN0_N	10
11	RESIN_N	IN1_N	12
13	USB_VCC	USB_D+	14
15	USB_GND	USB_D-	16
17	SGND	SGND	18
19	CTS_0	RTS_0	20
21	RXD_0	TXD_0	22
23	SGND	SGND	24
25	RXD_1-	TXD_1-	26
27	RXD_1+	TXD_1+	28
29	ETH_GND	ETH_GND	30
31	ETH_RX+	ETH_TX+	32
33	ETH_RX-	ETH_TX-	34
35	SGND	SGND	36
37	SCL	SDA	38
39	rsvd	SGND	40
41	SGND	rsvd	42
43	PRGIO0	SGND	44
45	PRGIO1	PRGIO2	46
47	SGND	PRGIO3	48
49	PRGIO4	PRGIO5	50
51	PRGIO6	SGND	52
53	PRGIO7	PRGIO8	54
55	SGND	PRGIO9	56
57	PRGIO10	PRGIO11	58
59	PRGIO12	SGND	60
61	PRGIO13	PRGIO!4	62
63	SGND	PRGIO15	64

BUS 2

Pin	Signal	Signal	Pin
1	AVCC-	AVCC-	2
3	AVCC+	AVCC+	4
5	AGND	AGND	6
7	GPIO2	GPIO3	8
9	D0 *1	D1 *1	10
11	D2 *1	D3 *1	12
13	SGND	D4 *1	14
15	D5 *1	D6 *1	16
17	D7 *1	SGND	18
19	D8 *1	D9 *1	20
21	SGND	D10 *1	22
23	D11 *1	D12 *1	24
25	D13 *1	SGND	26
27	D14 *1	D15 *1	28
29	SGND	A6 *1	30
31	A7 *1	A8 *1	32
33	A9 *1	SGND	34
35	A10 *1	A11 *1	36
37	SGND	A12 *1	38
39	A13 *1	A14 *1	40
41	A15 *1	SGND	42
43	BE0_N *1	BE1_N *1	44
45	SGND *1	DATR0 *1	46
47	CLKR0 *1	FSR0 *1	48
49	DATX0 *1	SGND *1	50
51	CLKX0 *1	FSX0 *1	52
53	SGND	DATR1	54
55	CLKR1	FSR1	56
57	DATX1	CLKX1	58
59	FSX1	RESOUT_N	60
61	GND_OUT	GND_OUT	62
63	VCC_OUT	VCC_OUT	64

greyed signals are not connected to the FPGA but inter-connected on top and bottom connectors

*1 split signal: top and bottom connector routed to individual FPGA pins

*2 signals can be disconnected from top connector

SGND = signal return ground, do not use for power supply

EXP

Pin	Signal	Signal	Pin
1	SGND		2
3			4
5		SGND	6
7			8
9	SGND		10
11			12
13		SGND	14
15			16
17	SGND		18
19			20
21		SGND	22
23			24
25	SGND		26
27			28
29		SGND	30
31			32
33	SGND	D0_P *2	34
35	D1_P *2	D0_M *2	36
37	D1_M *2	SGND	38
39	CLK1_M *2	CLK1_P *2	40
41	SGND	D2_P *2	42
43	D3_P *2	D2_M *2	44
45	D3_M *2	SGND	46
47	CTL1_M *2	CTL1_P *2	48
49	SGND	D4_P *2	50
51	D5_P *2	D4_M *2	52
53	D5_M *2	SGND	54
55	CLK2_M *2	CLK2_P *2	56
57	SGND	D6_P *2	58
59	D7_P *2	D6_M *2	60
61	D7_M *2	SGND	62
63	CTL2_M *2	CTL2_P *2	64

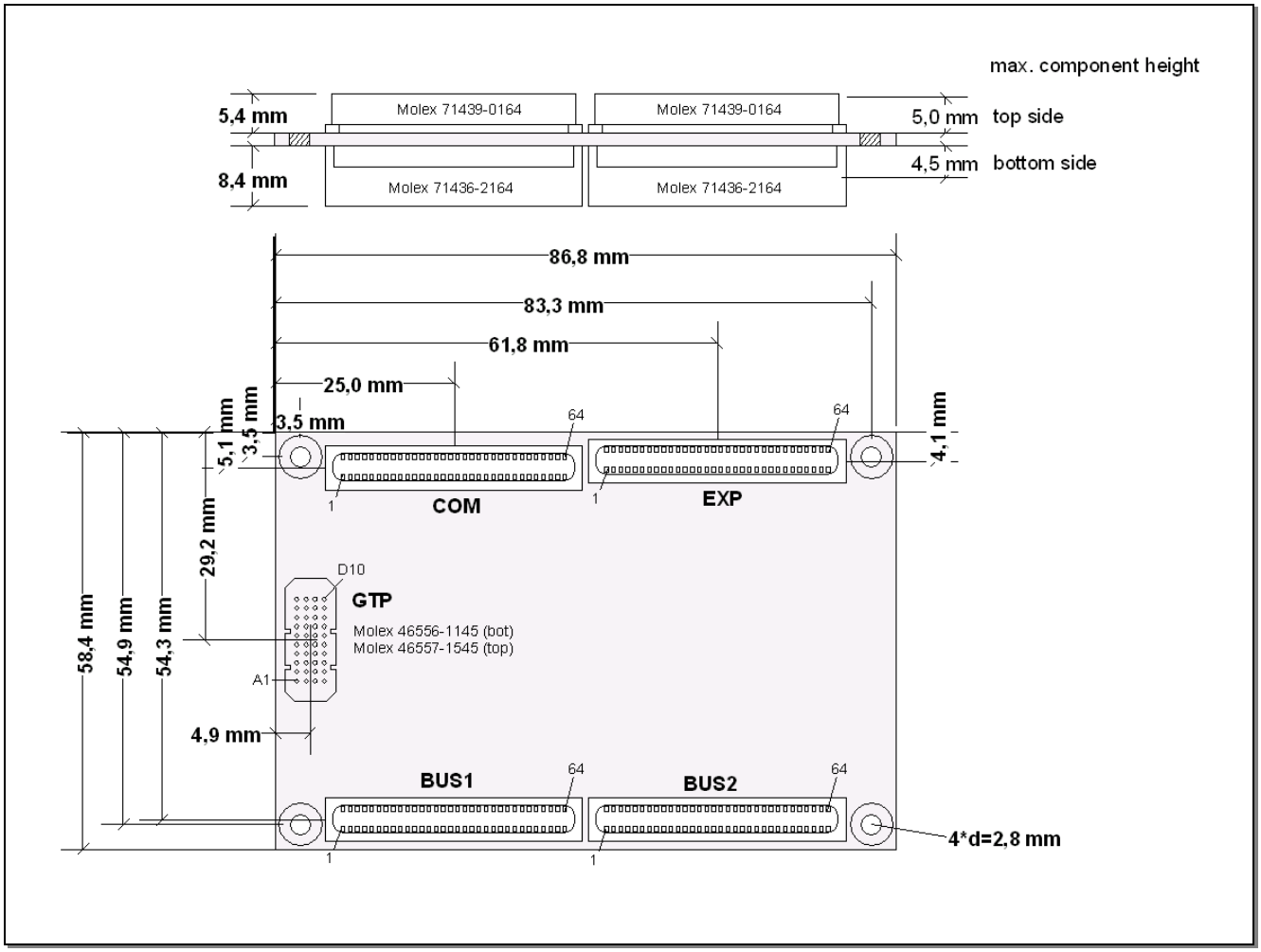
GTP Top

	A	B	C	D
1	SGND	SGND	nc	SGND
2	DSP_PETp0	SGND	SGND	TX1P
3	DSP_PETn0	nc	nc	TX1N
4	SGND	nc	nc	SGND
5	DSP_PERp0	SGND	SGND	RX1P
6	DSP_PERn0	nc	nc	RX1N
7	SGND	nc	nc	SGND
8	DSP_REFCLKp	SGND	SGND	nc
9	DSP_REFCLKn	nc	SGND	nc
10	SGND	nc	nc	SGND

GTP bottom

	A	B	C	D
1	SGND	SGND	GPIO0	SGND
2	DSP_PETp0	SGND	SGND	PETp0
3	DSP_PETn0	RX2P	RX3P	PETn0
4	SGND	RX2N	RX3N	SGND
5	DSP_PERp0	SGND	SGND	PERp0
6	DSP_PERn0	TX2P	TX3P	PERn0
7	SGND	TX2N	TX3N	SGND
8	DSP_REFCLKp	SGND	SGND	REFCLKp
9	DSP_REFCLKn	CLK2P	SGND	REFCLKn
10	SGND	CLK2N	GPIO1	SGND

MECHANICAL DIMENSIONS



ORDERING INFORMATION

D.Module2.6SLX45T	with XC6SLX45T FPGA
D.Module2.6SLX100T	with XC6SLX100T FPGA
DS.6SLX45T	Development Support Base Package including documentation, Xilinx ISE project files, DSP bus interface examples (VHDL and C code), DSP source code for Configuration Flash updates, etc.
D.Module2.Base-FMC	FPGA, DSP and FMC Mezzanine Carrier and Prototyping Platform
Tools	download the free Xilinx WebPack ISE software suite from www.xillinx com

Additional Options On Volume Purchase

For volume purchase D.SignT offers customer specific modifications of the hardware either to reduce costs through reduced functionality or to increase functionality to meet the customers application requirements. Extensive experience in custom designs and the powerful engineering tools of our development department bring your application and our DSP know how together for your solution. Please contact D.SignT directly.

Technical Support

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Pricing

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Availability

Our standard D.Modules are available typically ex-stock. For special modifications or non-standard D.Module2 please consult our sales department.

Warranty

All D.Module2 boards come with a 12 month warranty .

For additional information contact your local distributor or D.SignT directly.

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