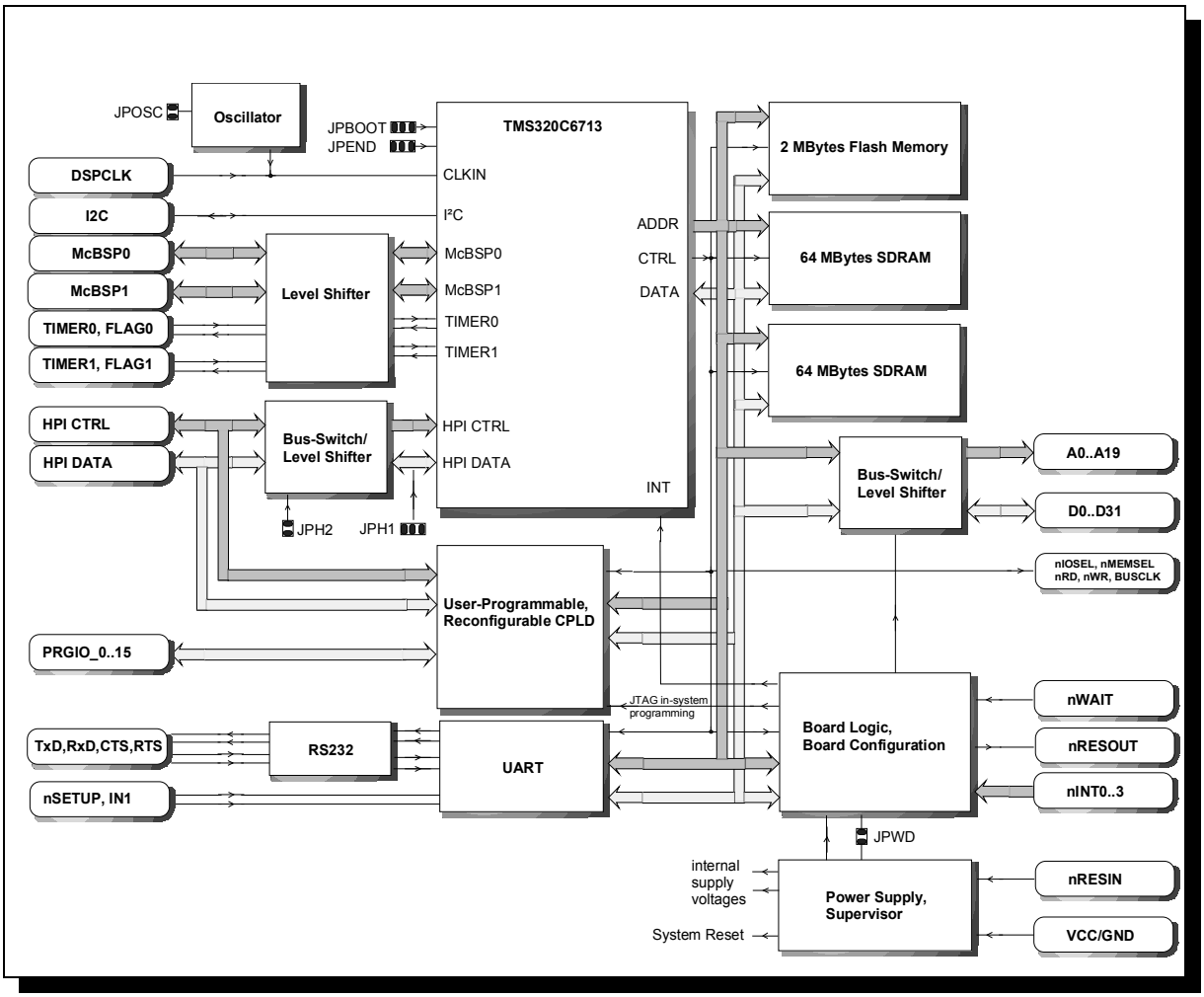
D.Module.C6713 Technical Data Sheet

- **Board Revision 3.0**

Document Revision 1.5 Oct 2012

SUMMARY

- **Highest Performance Floating Point DSP Computer Module, based on TMS320C6713B**
- **Peak Performance 2400 MIPS, 1800 MFLOPS**
- **Stand-alone Operation**
- **Watchdog and Power Supply Supervisor**
- **Two Level Cache Architecture**
- **2 Mbytes non-volatile Flash Memory**
- **128 Mbytes SDRAM**
- **3.3V Single Supply**
- **Two 5V tolerant Serial Ports**
- **I²C Bus**
- **External Bus Interface for memory and I/O expansion (5V tolerant)**
- **Wait State Logic**
- **Two pre-decoded Memory Select Signals**
- **UART with FIFOs and Auto-Flow Control, RS232 line interface**
- **User configurable 72 macrocell CPLD for I/O expansion and interface adaptation, 16 free I/Os (42 if HPI not used)**
- **16 Bit wide, 5V tolerant Host Port Interface, also usable as an Expansion Port for high-speed data acquisition**
- **D.Module.BIOS, Configuration and Set-Up Utility**
- **Two 32 bit Timers**
- **Four external Interrupts**
- **JTAG Emulator Port**
- **Small Size: only 85 x 59 mm**



The D.Module family of DSP based Computer Modules offers a standardized hardware platform for embedded DSP applications. Mechanics and pinout are identical throughout the family members. 111 signals are reserved and provide identical functionality. In combination with the D.Module.BIOS - a hardware independent application programming interface for onboard components UART, Flash Mem-

ory etc. - portability is maintained. Adaptation is reduced to a minimum if your system's requirements change.

DSP

The heart of the D.Module.C6713 is the advanced VLIW architecture floating point digital signal processor TMS320C6713 from Texas Instruments. This RISC architecture DSP provides 8 instruction units which operate in parallel, yielding a maximum performance of 2400 MIPS, 1800 MFLOPS. Up to 256 Kbytes internal memory and a two level cache architecture (64 Kbytes L2 cache, 4 Kbytes L1 program cache and 4 Kbytes L1 data cache) guarantee the memory bandwidth required to sustain high data throughput. Furthermore, two multichannel buffered synchronous serial ports, an I2C bus interface, two timers, an enhanced DMA controller and a 16 bit wide Host Interface are built into this processor.

The multichannel buffered serial ports provide a direct connection to T1/E1, SCSA, MVIP, AC-97, ST-Bus and SPI interfaces, and industry standard Codecs, A/D and D/A converters. High Speed data transfer up to 75 MBits/sec is possible. This also provides an efficient data path for multiprocessor communications.

The built-in DMA controller provides enhanced features for 1D and 2D transfers and auto-initialization, which allows to maintain circular and ping-pong buffers without any CPU intervention.

MEMORY

The DSP itself provides up to 256 Kbytes internal memory, usable as program and/or data memory. 64 Kbytes of this memory area can be configured as a 4-way second level cache to increase throughput if large data structures or program code reside in external memory.

Additionally two banks of 64 Mbytes on-board SDRAM can be used for large data buffers as commonly required by image processing applications. Byte, Halfword and Word data is supported. SDRAM also operates at 100 MHz.

Two Mbytes Flash Memory are integrated for non-volatile data and program storage. The Flash Memory is divided in multiple sectors of 64 Kbytes. Each sector can be erased individually and (re-)programmed on a Byte basis. The DSP has direct access to the Flash Memory: Identification, Sector-Erase and Programming is handled by BIOS functions which effectively encapsulate the programming algorithms.

Further external memory expansion is possible using the two pre-decoded select signals. The IOSEL and MEMSEL memory ranges are primarily intended to connect parallel interface data acquisition and communication devices, but can be used for memory expansion too: IOSEL only supports asynchronous devices, but MEMSEL also supports external SDRAM expansions.

CLOCKS

An on board oscillator generates the DSP master clock. Additional clocks for external peripherals can be generated using the two 32 bit timers. The Serial Ports feature their own clock generation circuitry based on the DSP clock or an external master clock.

POWER SUPPLY

The D.Module.C6713 requires a 3.3V single voltage power supply only. Secondary voltages for RS232 and CPU core are generated on board using PWM regulators and charge pumps. A micro-processor supervisor circuit controls the power supply sequencing and holds the board in reset if the supply voltage is below it's limit.

EXTERNAL BUS INTERFACE

The external bus interface is fully 5V tolerant to support a direct connection to 5V environments. The data bus is 32 bit wide, 20 address lines and four byte select outputs provide access to a linear 256 Mbytes address range (MEMSEL) and a 1 Mbyte linear address range for I/O expansion (IOSEL). The bus interface timing is independently programmable for both memory areas. Peripherals connected to the external bus interface can request additional wait states or delay a bus cycle using the nWAIT input. The minimum I/O cycle time is 20 nsecs.

UART

The UART offers powerful features: 32 word receive and transmit FIFOs, automatic flow control (RTS/CTS and Xon/Xoff), and DMA support relieve the DSP from time-consuming interrupt driven data transfers. Baud rates up to 460 kBaud are possible. The line interface is RS232, optionally RS422/485 is available. The onboard wait state logic generates the required wait states for UART accesses while retaining fast access to other asynchronous memory devices or expansions. The UART is fully sup-

ported by the D.Module.BIOS: initialization and communication functions are provided

USER-CONFIGURABLE CPLD

One of the major challenges in DSP design is the integration into a host system and interfacing peripherals. To facilitate this, the D.Module.C6713 integrates a high speed 72 macrocell in-system programmable CPLD. 16 bit databus, address lines, control and clock signals are pre-connected to the DSP. The CPLD can be re-programmed via the module's Set-Up Utility by uploading the programming file.

Additional I/O ports, serial interfaces, bus interface adaptation, PWM and clock generation are some of the most typical applications. 16 I/Os are available and can be configured as input, output, or bi-directional signals. If the Host Port Interface is not used 26 additional signals can be used for user-defined I/O.

HOST INTERFACE

The 16 bit wide TMS320C6713 Host Port Interface is fully accessible on the D.Module. A host controller has direct access to the entire memory range of the DSP. The HPI is 5V tolerant and multiplexed with User-CPLD signals. This configuration allows the User-CPLD to control the HPI, or expand the number of user-programmable I/O if the HPI is not used. With the help of the User-CPLD, the Host Port Interface can also be used as a 16 bit wide expansion port to provide a high-speed path for fast data acquisition, separated from the external memory interface. Background data transfers via the HPI are possible while leaving the full external memory interface bandwidth to the CPU.

BOOT OPTIONS

By default the D.Module.C6713 is bootloaded from the Flash Memory. In this mode the BIOS, Configuration Utility and the Set-Up Utility are loaded first. The nSETUP signal (IN0) is sampled, if low Set-Up Mode is entered which allows to store programs and data in the Flash Memory, program the CPLD and execute diagnostic functions via a RS232 terminal connection. If nSETUP is not asserted, the BIOS bootloader loads the application program and executes it. Bootloading via the HPI is also supported.

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MODULE CONFIGURATION

A module configuration register controls additional I/O signals on the D.Module.C6713: Watchdog-Trigger, Reset-Output and Interrupt Multiplexer. Solder links are used to set the boot mode.

The D.Module.C6713 provides a unique Module Configuration File which is permanently stored in the Flash Memory. The Configuration File allows to store human-readable ASCII data for configuration such as communication parameters, signal-processing coefficients, temperature compensation tables etc. Maintenance and modifications of installations is greatly simplified: Edit the configuration file and upload the modified version in Set-Up mode.

The Module Configuration File also provides scripting mechanisms to control system start-up: selftest and calibration programs can be bootloaded and executed prior to the main application.

RESET and WATCHDOG

A micro-processor supervisor circuit monitors the power supply and resets the module during power-up, power-down and brown-out conditions.

A debounced external reset input can be used to connect a system reset signal or a push-button for manual reset. An open drain reset output is controlled via the module configuration register and can be used to initialize external peripherals.

A watchdog provides security against program lock-ups and hardware failures as required by most embedded applications. The watchdog timer must be re-triggered at least every 1.6 seconds, otherwise a reset is generated. The watchdog trigger is generated by the module configuration register. A status bit in the module configuration register reflects the cause of the last system reset. This allows to distinguish normal power-on or manual reset from a watchdog timeout.

EXTERNAL INTERRUPTS

The D.Module.C6713 provides four external 5V tolerant interrupt inputs. Interrupts are edge triggered and can be configured for falling or rising edge. These inputs are multiplexed with CPLD and UART interrupts and UART DMA requests, controlled via the module configuration register.

BIOS

The D.Module.BIOS is an application programming interface for all on board resources. It encapsulates the hardware dependencies and provides functions for

- Module initialization
- UART initialization , send and receive functions
- Flash Memory programming support: identify device, erase a sector, programming and reading bytes, halfwords and words
- Module configuration: set and clear bits and bitfields in the module configuration register
- Miscellaneous functions: bootload and delay.
- Low-Level device drivers for stdio access (fprintf, fscanf etc.) to the UART and Flash Memory
- Functions to read parameters and settings from the Module Configuration File

These functions are identical on all D.Modules and help to maintain program portability throughout the D.Module family. The BIOS is written in hand-coded Assembler language to achieve optimum performance. All functions are C callable.

SET-UP MODE

By holding the nSETUP input low at system reset the module will enter Set-Up mode. In this mode the board communicates via a terminal connection and provides several options to upload programs, parameters and configuration files to the Flash Memory, re-program the User-CPLD, invoke test programs and basic debugging features - without the need for special programming or emulation equipment.

MEMORY MAP

DSP Address	Memory	Wait States	Description
0x0000.0000..0x0000.01FF	internal	0	512 Bytes Interrupt Vector Table
0x0000.0200..0x0000.11FF			4 Kbytes D.Module.BIOS Functions
0x0000.1200..0x0002.FFFF			187.5 Kbytes mapped L2 RAM, free for user application
0x0003.0000..0x0003.FFFF			64 Kbytes mapped L2 RAM (free for user application) or 4-way L2 cache
0x0180.0000..0x3C1F.FFFF	-	-	DSP built-in peripherals
0x8000.0000..0x83FF.FFFF	SDRAM 1	0	64 Mbytes on-board SDRAM, free for user application
0x9000.0000..0x901F.FFFC	Flash Memory	CE1, auto	2 Mbytes on-board Flash Memory in four banks of 512 Kbytes , bank select via the Module Configuration Register
0x9020.0000..0x9020.003C	User-CPLD	CE1, auto	User-programmable CPLD, pre-connected to DSP data and address bus
0x9028.0000..0x9028.000C	Module Cfg	CE1, auto	Module Configuration Registers
0x902C.0000..0x902C.001C	UART	CE1, auto	UART
0x9030.0000..0x903F.FFFC	IOSEL	CE1	IOSEL memory area, nIOSEL is driven low if access inside this memory area, 32 bit wide asynchronous access
0xA000.0000..0xAFFF.FFFF	MEMSEL	CE2	MEMSEL memory area, nMEMSEL is driven low if access inside this memory area, supports and SDRAM memories
0xB000.0000..0xB3FF.FFFF	SDRAM 2	0	64 Mbytes on-board SDRAM, free for user application

BOARD CONFIGURATION REGISTER

RESETS (Addr. 0x9028.0000)

Bit	Function	Reset State	Description
0	RES_SOURCE	see text	source of the last system reset, read only 1 - Reset by watchdog timeout 0 - Reset by power-on or manual reset
1	nRESOUT	0	controls the nRESOUT pin U7 1 - nRESOUT = high 0 - nRESOUT = low (default after reset)
2	CPLD_WAIT	0	enable external wait state requests via nWAIT on access to the User-CPLD 1 - read nWAIT on CPLD access 0 - ignore nWAIT on CPLD access (default after reset)
3	UART_RESET	1	reset the UART 1 - UART in reset (default after reset) 0 - UART in normal operation
4	CPLD_RESET	0	reset the User-CPLD 1 - User-CPLD in normal operation 0 - User-CPLD in Reset (default after reset)
5	WDOG_TRIG	0	watchdog trigger 1 - toggle watchdog trigger each time a '1' is written to this bit 0 - watchdog trigger remains unchanged

INTERRUPT MULTIPLEXER (Addr. 0x9028.0004)

Bit	Function	Reset State	Description
0	INT5_MUX	0	mapping of DSP interrupt INT5 0 - external interrupt nINT1 (Pin U4) 1 - User-CPLD interrupt
2,1	INT6_MUX	00	mapping of DSP interrupt INT6 00 - external interrupt nINT2 (Pin A19) 01 - User-CPLD interrupt 10 - UART interrupt 11 - UART receive DMA request
4,3	INT7_MUX	00	mapping of DSP interrupt INT7 00 - external interrupt nINT3 (Pin A20) 01 - User-CPLD interrupt 10 - UART interrupt 11 - UART transmit DMA request

FLASH MEMORY BANK SELECT REGISTER (Addr. 0x9028.0008)

Bit	Function	Reset State	Description
0,1	FLASH_BANK	00	Flash Memory Bank Select, maps the given 512 Kbytes Flash Memory Bank to DSP address space 0x9000.0000. Setting the Flash Memory Bank is automatically handled by the D.Module.BIOS Flash Memory functions

MISCELLENEAOUS REGISTER (Addr. 0x9028.000C)

This register controls the User-CPLD in-system JTAG programming port and reads factory setting configuration jumpers. Not to be accessed by user application.

SIGNAL DESCRIPTION

POWER SUPPLY

Signal	Pin	Type	Description
VCC	A1, B32	PWR	positive power supply, 3.3V
GND	B1, A32	PWR	ground, 0V
+AVCC	C17, U1	-	these signals are not connected on the D.Module.C6x01, use to route analogue supply voltage to daughter cards
AGND	C16, U32		
-AVCC	C15, U31		

DSP PERIPHERALS

Signal	Pin	Type	Description
TIMER0	A21	O	Timer 0 output
TIMER1	A22	O	Timer 1 output
FLAG0	A23	I	Timer 0 input
FLAG1	A24	I	Timer 1 input
CLKS0	A25	I	McBSP 0 external master clock input
DAT_RX0	A26	I	McBSP 0 receiver data input
CLK_RX0	A27	I/O	McBSP 0 receiver clock
FS_RX0	A28	I/O	McBSP 0 receiver frame sync
DAT_TX0	A29	I	McBSP 0 transmitter data output
CLK_TX0	A30	I/O	McBSP 0 transmitter clock
FS_TX0	A31	I/O	McBSP 0 transmitter frame sync
CLKS1	B25	I	McBSP 0 external master clock input
DAT_RX1	B26	I	McBSP 1 receiver data input
CLK_RX1	B27	I/O	McBSP 1 receiver clock
FS_RX1	B28	I/O	McBSP 1 receiver frame sync
DAT_TX1	B29	I	McBSP 1 transmitter data output
CLK_TX1	B30	I/O	McBSP 1 transmitter clock
FS_TX1	B31	I/O	McBSP 1 transmitter frame sync
SDA0	A17	I/O	I²C Bus Interface data, open drain NOT 5V TOLERANT!
SCL0	A18	I/O	I²C Bus Interface clock, open drain NOT 5V TOLERANT!

EXTERNAL INTERRUPTS

Signal	Pin	Type	Description
nINT0	U3	I	on-board pull-up 10K
nINT1	U4	I	via Interrupt Multiplexer in Module Config Register, on-board pull-up 10K
nINT2	A19	I	via Interrupt Multiplexer in Module Config Register, on-board pull-up 10K
nINT3	A20	I	via Interrupt Multiplexer in Module Config Register, on-board pull-up 10K

MISCELLANEOUS SIGNALS

Signal	Pin	Type	Description
DSPCLK	A7	I	external clock if JPOSC closed NOT 5V TOLERANT!
IN0(nSETUP)	A11	I	UART DSR, on-board 10K pull-up NOT 5V TOLERANT!
IN1	A12	I	UART RI, on-board 10K pull-up NOT 5V TOLERANT!
nRESIN	A9	I	debounced manual reset, on-board pull-up 10K
nRESOUT	U7	O	reset output, active low

UART

Signal	Pin	Type	Description
RTS	A2	O	RS232 Request To Send (Handshake), RS422 Transmit Data inverted
TxD	A3	O	Transmit Data
CTS	A4	I	RS232 Clear To Send (Handshake), RS422 Receive Data inverted
RxD	A5	I	Receive Data
GND	A6	PWR	RS232, RS422 Signal Ground

USER-PROGRAMMABLE CPLD

Signal	Pin	Type	Description
PRG_IO0	B2	I/O	user-configurable CPLD I/O
PRG_IO1	B3	I/O	user-configurable CPLD I/O
PRG_IO2	B4	I/O	user-configurable CPLD I/O
PRG_IO3	B5	I/O	user-configurable CPLD I/O
PRG_IO4	B6	I/O	user-configurable CPLD I/O
PRG_IO5	B7	I/O	user-configurable CPLD I/O
PRG_IO6	B8	I/O	user-configurable CPLD I/O
PRG_IO7	B9	I/O	user-configurable CPLD I/O
PRG_IO8	B10	I/O	user-configurable CPLD I/O
PRG_IO9	B11	I/O	user-configurable CPLD I/O
PRG_IO10	B12	I/O	user-configurable CPLD I/O
PRG_IO11	B13	I/O	user-configurable CPLD I/O
PRG_IO12	B14	I/O	user-configurable CPLD I/O
PRG_IO13	B15	I/O	user-configurable CPLD I/O
PRG_IO14	B16	I/O	user-configurable CPLD I/O
PRG_IO15	B17	I/O	user-configurable CPLD I/O

HOST PORT INTERFACE

Signal	Pin	Type	Description
HD0..HD15	T15..T30	I/O	Host Port D0 .. D15 or User-CPLD I/O
nHCS	T31	I	Host Chip Select or User-CPLD I/O
HHWIL	T12	I	Host 1st/2nd Halfword or User-CPLD I/O
HCNTL0	T13	I	Host Register Select Line 0 or User-CPLD I/O
HCNTL1	T14	I	Host Register Select Line 1 or User-CPLD I/O
nHRDY	B18	O	Ready to Host or User-CPLD I/O
nHINT	B19	O	Interrupt to Host
nHAS	B20	I	Host Address Strobe or User-CPLD I/O
nHDS1	B21	I	Host Data Strobe 1 or User-CPLD I/O
nHDS2	B23	I	Host Data Strobe 1 or User-CPLD I/O
HRnW	B22	I	Host Read/Write Direction or User-CPLD I/O
HNC	B24	I/O	not connected to Host Port, User-CPLD I/O provided for compatibility with D.Module.C6701

EXTERNAL BUS INTERFACE

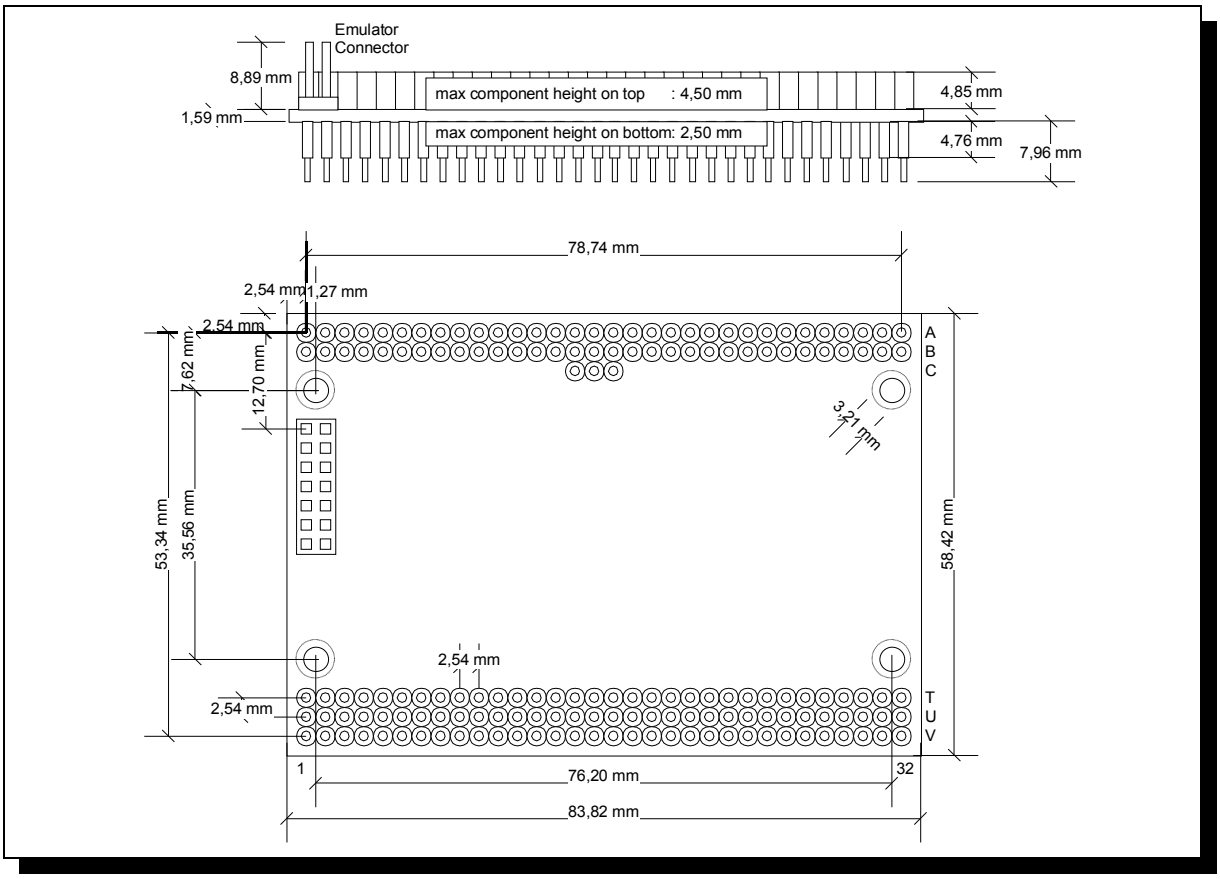
Signal	Pin	Type	Description
D0..D15	V15..V30	I/O	ext. Data Bus D0 .. D15
D16..D31	U15..U30	I/O	ext. Data Bus D16 .. D31
A0..A5	U9..U14	O	ext. Address Bus , DSP EA2 .. EA7
A6..A18	V2..V14	O	ext. Address Bus , DSP EA8 .. EA20
A19	A14	O	ext. Address Bus , DSP EA21
nRD	U2	O	Read Strobe, active low
nWR	U5	O	Write Strobe, active low
nIOSEL	U8	O	IOSEL Memory Select, active low
nMEMSEL	V31	O	MEMSEL Memory Select, active low
BUSCLK	U6	O	DSP ECLKOUT external memory interface clock
nWAIT	A10	I	ext. Wait State Request, active low, on-board pull-up 10K
SDCLK	T2	O	DSP ECLKOUT external memory interface clock
nAOE / nSDRAS	T3	O	asynchronous output enable or SDRAM row address strobe, active low. use this signal to control the direction of external bus transceivers or for external SDRAM memory expansions
nSDCAS	T4	O	ext. SDRAM column address strobe, active low
nSDWE	T5	O	ext. SDRAM write enable, active low
SDA10	T6	O	ext. SDRAM address line A10
nCE3	T7	O	DSP /CE3 chip select line, active low, use only if no on-board SDRAM

nBE0..nBE3	T8..T11	O	Byte Enable 0 .. 3, active low
nHOLD	A15	I	ext. bus hold request, active low NOT 5V TOLERANT!
nHOLDA	A16	O	ext. bus hold acknowledge

PINOUT

Pin	A	B	C	T	U	V
1	VCC	GND		nc	+AVCC	nc
2	RTS / nTxD	PRG_IO0		SDCLK	nRD	A6
3	TxD	PRG_IO1		nSDRAS / nAOE	nINT0	A7
4	nc / nRxD	PRG_IO2		nSDCAS	nINT1	A8
5	RxD	PRG_IO3		nSDWE	nWR	A9
6	GND	PRG_IO4		SDA10	BUSCLK	A10
7	DSPCLK	PRG_IO5		nSDCS	nRESOUT	A11
8	GND	PRG_IO6		nBE0	nIOSEL	A12
9	nRESIN	PRG_IO7		nBE1	A0	A13
10	nWAIT	PRG_IO8		nBE2	A1	A14
11	IN0 / nSETUP	PRG_IO9		nBE3	A2	A15
12	IN1	PRG_IO10		HHWIL	A3	A16
13	GND	PRG_IO11		HCNTL0	A4	A17
14	A19	PRG_IO12		HCNTL1	A5	A18
15	nHOLD	PRG_IO13	-AVCC	HD0	D16	D0
16	nHOLDA	PRG_IO14	AGND	HD1	D17	D1
17	SDA0	PRG_IO15	+AVCC	HD2	D18	D2
18	SCL0	nHRDY		HD3	D19	D3
19	nINT2	nHINT		HD4	D20	D4
20	nINT3	nHAS		HD5	D21	D5
21	TIMER0	nHDS1		HD6	D22	D6
22	TIMER1	HRnW		HD7	D23	D7
23	FLAG0	nHDS2		HD8	D24	D8
24	FLAG1	HNC		HD9	D25	D9
25	CLKS0	CLKS1		HD10	D26	D10
26	DAT_RX0	DAT_RX1		HD11	D27	D11
27	CLK_RX0	CLK_RX1		HD12	D28	D12
28	FS_RX0	FS_RX1		HD13	D29	D13
29	DAT_TX0	DAT_TX1		HD14	D30	D14
30	CLK_TX0	CLK_TX1		HD15	D31	D15
31	FS_TX0	FS_TX1		nHCS	-AVCC	nMEMSEL
32	GND	VCC (3.3V)		GND	AGND	GND

MECHANICAL DIMENSIONS



- Size: max. 85 x 59 x 15 mm
- Weight: 58g (2.05oz)

ELECTRICAL CHARACTERISTICS

OPERATING CONDITIONS, DC PARAMETERS

Supply Voltage VCC	3.3V +/- 5%
Power Consumption	idle 240mA (in reset), typ. 500mA, max. 1.5A
Operating Temperature	0..+70°C
High Level Input Voltage	min. 2V, max. VCC+0.2V
Low Level Input Voltage	min. -0.2V, max. 0.8V

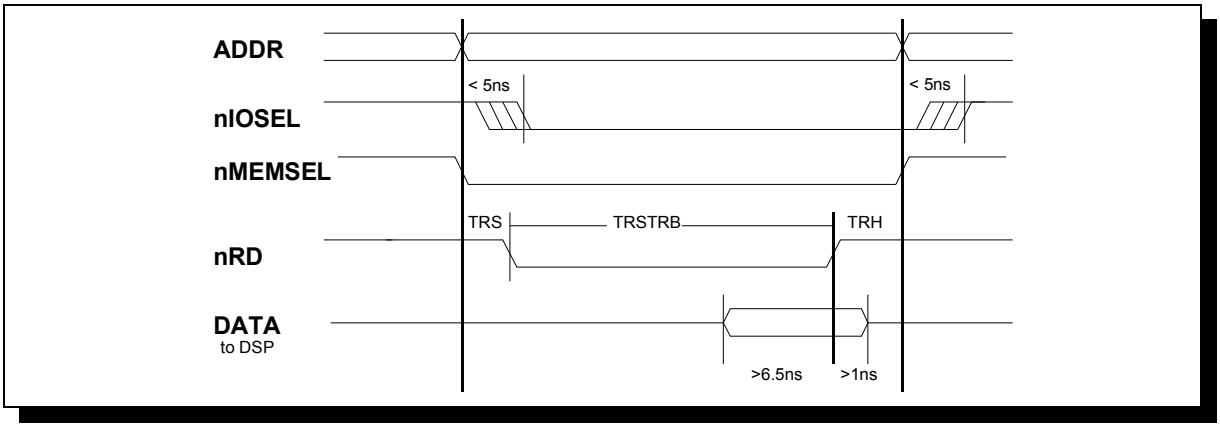
Power Consumption largely depends on the application program, i.e the amount and frequency of external bus and memory accesses and the utilisation of DSP resources. The idle power consumption is measured while the module is held in reset, the maximum value is calculated based on Texas Instruments data sheet information and experimental results.

TIMINGS

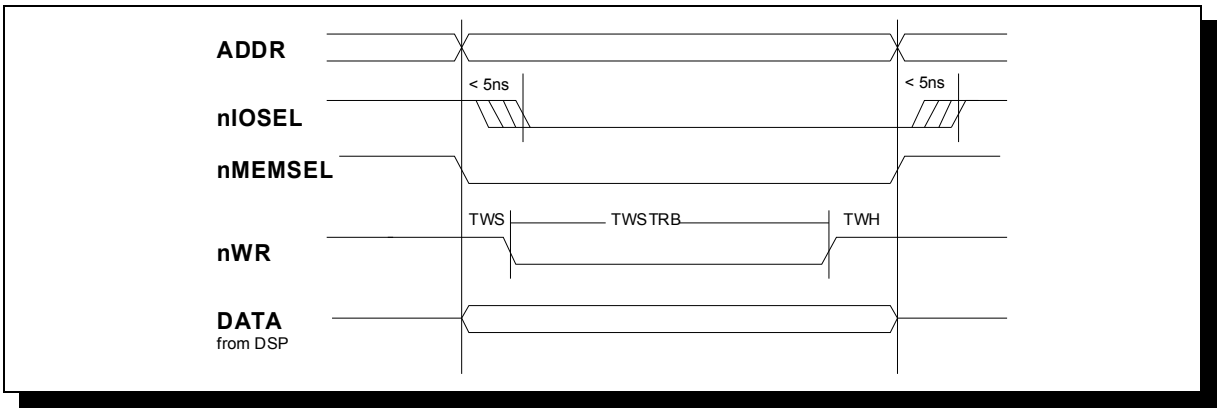
The external bus timings are shown in the following diagrams. For Serial Port and Host Port Interface timings please refer to the Texas Instruments TMS320C6713B data sheet.

EXTERNAL BUS TIMINGS

READ



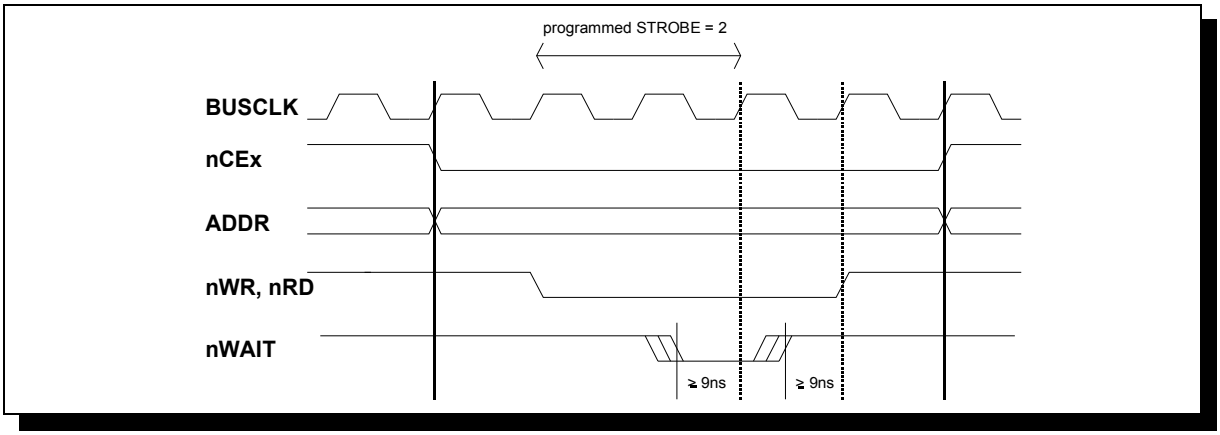
WRITE



TRS, TWS: read, write setup value programmed in CE1 rsp. CE2 Control Register
TRH, TWH: read , write hold value programmed in CE1 rsp. CE2 Control Register
TRSTRB, TWSTRB: read, write strobe value programmed in CE1 rsp. CE2 Control Register

Restrictions for nIOSEL (nCE1) : TRS, TWS >= 1, TRSTRB, TWSTRB >= 2, TRH, TWH >= 1

WAIT



If external wait states should be requested, nWAIT must be driven low at least 9 ns before the end of the programmed strobe time (TRSTRB, TWSTRB). The strobe cycle will end on the next rising BUSCLK edge after nWAIT has returned to high level.

ORDERING INFORMATION

D.Module.C6713-300-D4	TMS320C6713 Floating Point DSP Computer Module 300 MHz operation, 2 Mbytes Flash Memory, 128 Mbytes SDRAM
D.Module.C6713-200I-D4	industrial grade module, 200 MHz operation
Option -422	RS422 UART Line Interface
DS.C671x	Development Board Support Package Support Software, BIOS license, CPLD library, Boot-Code Generation Utility, Base Board, Power Supply, User's Guide and BIOS Reference Manual
TMDSCCS-ALLxxx	Texas Instruments TMS320C6000 Code Composer Studio IDE (Code Generation Tools, Debugger, and Utilities)
701900	Spectrum Digital portable JTAG Emulator, connected via USB port
701905	Spectrum Digital high-speed USB2.0 JTAG Emulator
701910	Spectrum Digital isolated JTAG Emulator

ADDITIONAL OPTIONS ON VOLUME PURCHASE

For volume purchase D.SignT offers customer-specific modifications of the hardware either to reduce costs through reduced functionality or to increase functionality to meet the customers application requirements. Extensive experience in custom designs and the powerful engineering tools of our development department bring your application and our DSP know how together for your solution. Please contact D.SignT directly.

TECHNICAL SUPPORT

Our products include free of charge technical support. You can reach the technical support by e-mail (support@dsignt.de) phone or fax.

PRICING

Please ask for our current price list and volume discounts.

AVAILABLITY

Our standard D.Modules are available typically ex-stock. For special modifications or non-standard D.Modules please consult our sales department.

WARRANTY

All D.Modules come with a warranty of 12 month.

For additional information contact your local distributor or D.SignT directly.

Distributed and supported locally by

D.SignT GmbH & Co. KG

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D-47647 Kerken
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